GRINN

Datasheet

Grinn AstraSOM-261x

Getting Started Guide | Prebuilt Images | Developer Resources | Customer Support

1 Features

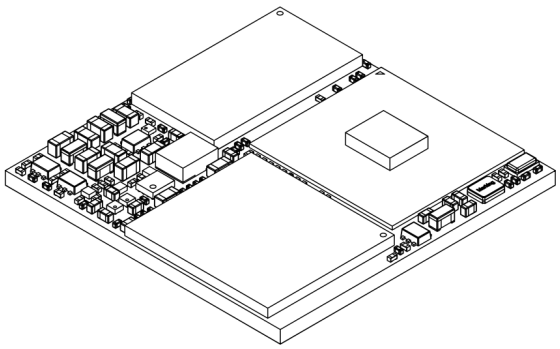
- Dual-core Arm® Cortex®-A55 SoC domain
- 1 TOPS Transformer-capable NPU
- Coral NPU based on RISC-V ML core
- 3D GPU: Arm® Mali®-G31
- MIPI-DSI up to 1080p60
- MIPI-CSI up to 2160p30
- Three TDM/I^{2}S interfaces with up to 16 audio channels
- Support for up to 8 digital microphones
- Hardware audio and camera mute support
- 2x USB 2.0 interfaces
- 2x SDIO 3.0 interfaces
- 4x TWSI (I^{2}C) interfaces
- 8x UART interfaces
- 1x SPIx interfaces
- Up to 96 GPIOs
- 11-bit ADC - 4 channels
- Up to 12 smart PWM modules in System Manager domain
- PSA Certified: Level 3 (Root of Trust), Level 2 (Product)
- Secure boot and true random number generator
- Cryptographic accelerators: RSA, AES, SHA, ECC, HASH
- 2x Gigabit Ethernet (RGMII) with Wake-on-LAN
- Up to 2GB 16 bit DDR4 RAM

2 Applications

- Multi-Camera Object Detection
- Natural Language Processing
- Medical Imaging and Analysis
- Autonomous Mobile Robots

3 Description

Grinn AstraSOM-261x is an end-to-end solution based on the Synaptics Astra SL2610 family, designed for power-efficient multimodal edge compute across a broad range of IoT and embedded systems. The platform integrates Arm® Cortex®-A55 application processors, a Cortex®-M52 System Manager domain, a Mali™ class 3D GPU, and dedicated neural processing units including the Torq™ T1 NPU and an integrated Coral NPU. Engineered for AI-native workloads, the Grinn AstraSOM-261x supports both transformer and convolutional neural network inference, enabling scalable deployment from battery-powered and passively cooled devices to high-performance industrial vision systems.



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4 Boot options

Grinn AstraSOM-261x can be booted from:

- xSPI
- eMMC
- USB

Boot devices are selected via physical pin configuration. `boot_src[0...1]` states are read after power-on and determine the boot flow. Pull-up or pull-down resistors should be used to drive these inputs to the appropriate state.

Tab. 1: Boot source pin mapping

SOM Pad	CPU Pin	Pin Name	CPU Pin Name	CPU Bias
L1	U26	`boot_src[0]`	`SM_GPIO8`	Pull-up
C17	G23	`boot_src[1]`	`SM_GPIO9`	Pull-down

Tab. 2: Boot source selection

boot_src[1:0]	Description
00b	ROM boot from USB2_0
01b	ROM boot from xSPI NOR [1]
10b	ROM boot from eMMC
11b	ROM boot from xSPI NAND

[1] Default boot configuration

4.1 System Software Strap

Pins `software_strap[3..0]` are used by software to recognize the hardware configuration of the board.

Tab. 3: Software strap pin mapping and default configuration

SOM Pad	CPU Pin	Pin Name	CPU Bias	SOM configuration
F2	B13	`software_strap[0]`	Pull-up	2.2 kΩ Pull-down
M18	AF27	`software_strap[1]`	Pull-down	2.2 kΩ Pull-up [1]
B3	C8	`software_strap[2]`	Pull-down	
D1	B9	`software_strap[3]`	Pull-down	

[1] Optional, check Tab. 4 for more details

Tab. 4: Software strap selection

software_strap[1]	Description
1b	RAM size = 2GB
0b	RAM size = 1GB

Note

- Pins `software_strap[1..0]` are configured on the SOM via 2.2 kΩ resistors and must not be modified.
- Pins `software_strap[3..2]` are reserved for future use and 2.2 kΩ pull-ups may be added in the future.

5 Functional Description

5.1 Hardware Resources

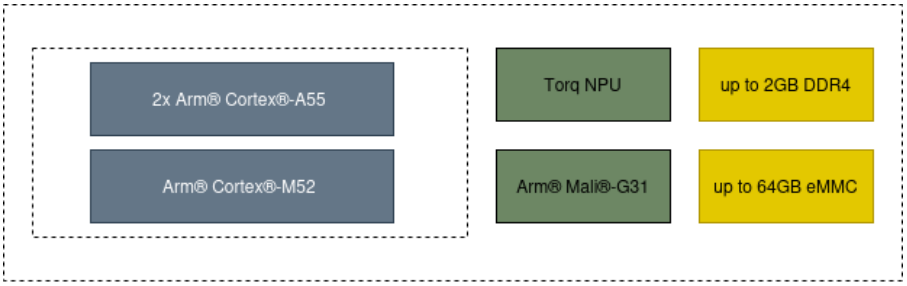


Fig. 1: Grinn AstraSOM-261x hardware resources overview

Grinn AstraSOM-261x is based on the SL261x high-performance edge AI SoC platform. It integrates Arm Cortex®-A55 application cores, a dedicated neural processing unit (NPU), graphics processing resources, multimedia engines, and embedded peripheral controllers required for edge AI and multimedia applications.

The SoC is supported by the SyNAP™ and Torq™ Edge AI software stacks, enabling developers to build, optimize, and deploy ML/AI applications for vision, audio, and multimodal processing at the edge.

Grinn AstraSOM-261x can be equipped with up to 2GB DDR4 RAM and up to 64GB eMMC Flash memory.

5.2 Power Architecture

The power management unit consists of 5 buck converters, one LDO and two load switches. **SOC_VCORE** is controlled via I2C (address 0x60). The Grinn AstraSOM-261x power supply uses four pads: **VSYS** (V1, V2, Y1, and Y2). All other power supplies are derived from **VSYS** using buck converters and LDO.

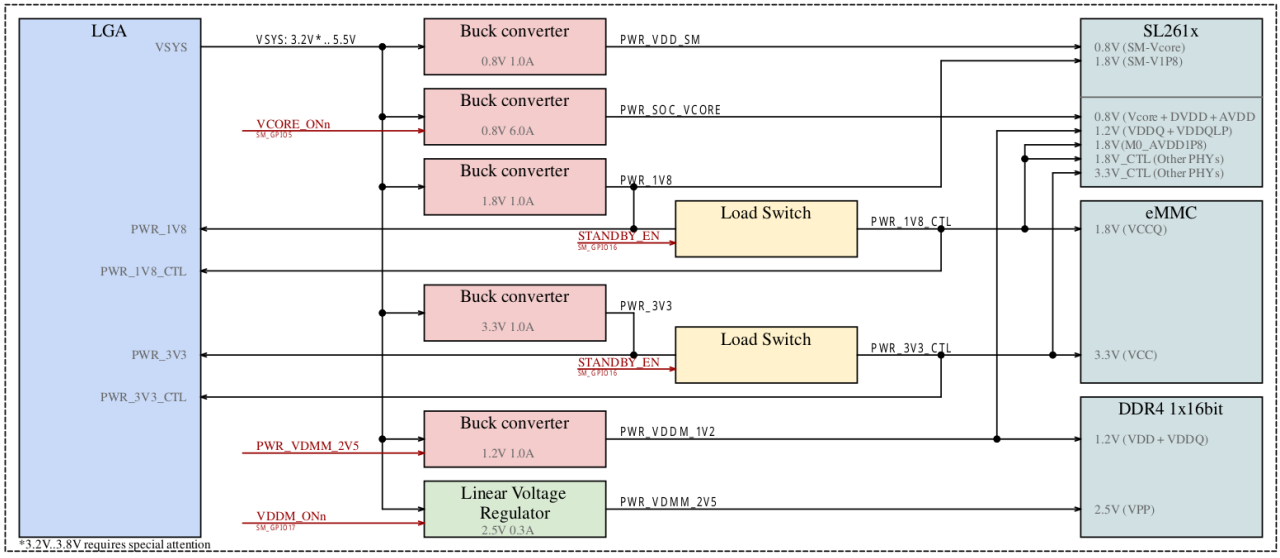


Fig. 2: Power supply routing

SOM is powered from a single **VSYS** input. Two output voltages are available to the user **PWR_1V8** and **PWR_3V3**. Each power rail has load switch integrated to provide **PWR_1V8_CTL** and **PWR_3V3_CTL** respectively.

- Active Mode: Both **PWR_1V8_CTL** and **PWR_3V3_CTL** are enabled, providing 1.8V and 3.3V respectively.
- Standby Mode: **PWR_1V8_CTL** and **PWR_3V3_CTL** are automatically disabled. However, the **PWR_1V8** and **PWR_3V3** rails remain available.

The **PWR_1V8** and **PWR_1V8_CTL** outputs share the same 1.8 V rail, and their combined current draw must not exceed 0.5 A. Similarly, the **PWR_3V3** and **PWR_3V3_CTL** outputs share the same 3.3 V rail, and their combined current draw must not exceed 0.5 A.

Tab. 5: Power supply pinout.

LGA Pad	CPU Pin	Signal Name
-	B24	PWR_VCORE_EN
-	N30	VDDM_ONn
T5	R29	STANDBY_EN

Warning

- If **VSYS** is in range 3.2V..3.8V, no external current should be drawn from **PWR_3V3** and **PWR_3V3_CTL**.
- **STANDBY_EN** is an output signal and must not be driven externally.

5.3 Interface Overview

Grinn AstraSOM-261x provides a broad set of interfaces for display, camera, audio, connectivity, and general-purpose system expansion.

- USB 2.0
- SPI
- UART
- I2C
- SDIO
- GPIO
- ADC
- sPWM
- PDM
- SPDIF
- ETH
- MIPI-DSI
- MIPI-CSI
- RGMII

5.3.1 Display and Camera Interfaces

The Synaptics SL261x processor family integrates a multimedia subsystem combining a GPU and a Neural Processing Unit (NPU). The GPU is based on the ARM Mali architecture and provides hardware acceleration for 2D/3D graphics through APIs such as OpenGL ES and Vulkan.

The integrated NPU accelerates deep learning inference workloads such as object detection, classification, and image segmentation. The heterogeneous architecture enables simultaneous camera capture via MIPI CSI, hardware video processing, and AI inference on the NPU.

Available display and camera interfaces:

- MIPI CSI camera interfaces
- MIPI DSI display interface

Tab. 6: Grinn AstraSOM-261x MIPI CSI pad description

LGA Pad	MCU Ball	Name	Pinmux	Delay (ps)
V8	AG15	CSI_D1_P	MIPI_CSI_D1p	103.70
V9	AH17	CSI_D0_P	MIPI_CSI_D0p	104.34
V11	AH19	CSI_CK_P	MIPI_CSI_CKp	117.79
Y8	AG16	CSI_D1_N	MIPI_CSI_D1n	103.83
Y9	AG17	CSI_D0_N	MIPI_CSI_D0n	104.11
Y11	AG19	CSI_CK_N	MIPI_CSI_CKn	118.05

Tab. 7: Grinn AstraSOM-261x MIPI DSI pad description

LGA Pad	MCU Ball	Name	Pinmux	Delay (ps)
V12	AG20	DSI_D3_P	MIPI_DSI_D3p	137.68
V14	AG22	DSI_D2_P	MIPI_DSI_D2p	102.42
V15	AF23	DSI_CK_P	MIPI_DSI_CKp	110.88
V17	AH24	DSI_D1_P	MIPI_DSI_D1p	95.67
V18	AG26	DSI_D0_P	MIPI_DSI_D0p	99.57
Y12	AG21	DSI_D3_N	MIPI_DSI_D3n	137.28
Y14	AH22	DSI_D2_N	MIPI_DSI_D2n	102.81
Y15	AF24	DSI_CK_N	MIPI_DSI_CKn	110.42
Y17	AG24	DSI_D1_N	MIPI_DSI_D1n	95.64
Y18	AH26	DSI_D0_N	MIPI_DSI_D0n	99.50

5.3.2 Audio Interfaces

Grinn AstraSOM-261x supports advanced audio processing use cases, including multi-channel audio capture, playback, and AI-assisted audio analysis. The platform enables audio pre-processing, neural-network-based inference, and post-processing for applications such as voice control, audio analytics, and multimedia playback.

Available audio interfaces:

- I2S input and output interfaces
- S/PDIF input or output
- PDM

Tab. 8: Audio interfaces pin description

LGG Pad	MCU Ball	Name	Pinmux	Delay (ps)
C19	D22	SM_GPIO37	SM_PDM_CLKIO	48.56
F17	V30	SM_GPIO0	SM_PDM_DI0	6.77
G17	AA29	GPIO1	I2S1_BCLK	6.76
G18	AA31	GPIO0	I2S1_LRCK	7.31
G19	W29	GPIO3	I2S1_MCLK	21.70
H17	AA30	GPIO2	I2S1_DO / SPDIFO	8.98
H18	AB30	GPIO4	I2S1_DI / SPDIFI	25.59
J17	U30	SM_GPIO2	SM_PDM_CLKIO / I2S2_MCLK	33.68
J19	B22	SM_GPIO38	SM_PDM_DI0	110.95
K18	AG29	GPIO18	PDM_DI2	52.05
L2	AA25	GPIO8	I2S2_DI / SPDIFI	167.07
L3	F19	SM_GPIO31	SM_PDM_DI0	190.77
L19	AF31	GPIO19	PDM_DI3	26.02
M2	AA26	GPIO7	I2S2_DO / SPDIFO / SM_PDM_CLKIO	175.14
N1	AC31	GPIO5	I2S2_LRCK / SPDIFI	191.21
P1	AC30	GPIO6	I2S2_BCLK / SPDIFO	174.56
R1	AD30	GPIO11	I2S2_MCLK / SM_PDM_CLKIO	173.37
T7	A21	SM_GPIO32	SM_PDM_CLKIO	241.17
T13	AC27	GPIO13	I2S3_BCLK / PDM_DI1	126.63
T14	AE24	GPIO12	I2S3_LRCK	98.45
U13	AF30	GPIO14	I2S3_DO / PDM_DI3 / SPDIFO	119.97
U14	AC25	GPIO15	I2S3_DI / SM_PDM_DI0 / SPDIFI	105.67
U17	AB28	GPIO9	PDM_DI1	94.38
Y5	AE30	GPIO10	PDM_DI2	201.19

5.3.3 USB

Grinn AstraSOM-261x provides two USB 2.0 interfaces on the LGA padout. Interface **USB2_0** exposes **D_P**, **D_N**, **ID**, and **VBUS**, while interface **USB2_1** exposes **D_P**, **D_N**, and **VBUS**. Dedicated **REXT** pins for both USB controllers are terminated on-module and are not routed to the carrier board. The carrier board layout should treat **D_P/D_N** as controlled-impedance differential pairs.

Tab. 9: Grinn AstraSOM-261x USB pad description

LGA Pad	MCU Ball	Name	Pinmux	Delay (ps)
H1	AD2	USB2_1_D_P	USB2_1_Dp	146.91
H2	AC2	USB2_1_D_N	USB2_1_Dn	146.98
H3	AC1	USB2_1_VBUS	USB2_1_VBUS	89.92
J1	AF2	USB2_0_D_P	USB2_0_Dp	116.33
J2	AE2	USB2_0_D_N	USB2_0_Dn	116.07
J3	AH2	USB2_0_ID	USB2_0_ID	89.13
K3	AH3	USB2_0_VBUS	USB2_0_VBUS	99.59

Note

The **USB2_x_VBUS** lines includes a 30 kΩ series resistor.

5.3.4 SDIO

Tab. 10: Grinn AstraSOM-261x SDIO pad description

LGA Pad	MCU Ball	Name	Pinmux	Delay (ps)
T9	AG13	SDIO_DATA1	SDIO_DATA1	138.54
T10	AH13	SDIO_DATA2	SDIO_DATA2	123.66
T11	AF12	SDIO_CLK	SDIO_CLK	104.97
U9	AF13	SDIO_DATA3	SDIO_DATA3	141.59
U10	AG12	SDIO_CMD	SDIO_CMD	145.53
U11	AF14	SDIO_DATA0	SDIO_DATA0	125.58

Note

The **SDIO_*** lines support 1.8V IO levels only.

5.3.5 Control and Miscellaneous Signals

Tab. 11: Grinn AstraSOM-261x miscellaneous control pad description

LGA Pad	MCU Ball	Name	Pinmux
F18	V31	SM_POR_EN	SM_POR_EN
J18	W30	SM_TCK	SM_TCK
M1	T29	SM_AUDIO_MUTE	SM_AUDIO_MUTE
P2	W25	CAMERA_MUTE	CAMERA_MUTE
P3	W26	SM_TRSTn	SM_TRSTn
Y6	U29	SM_RSTn	SM_RSTn

5.4 Pad Layout

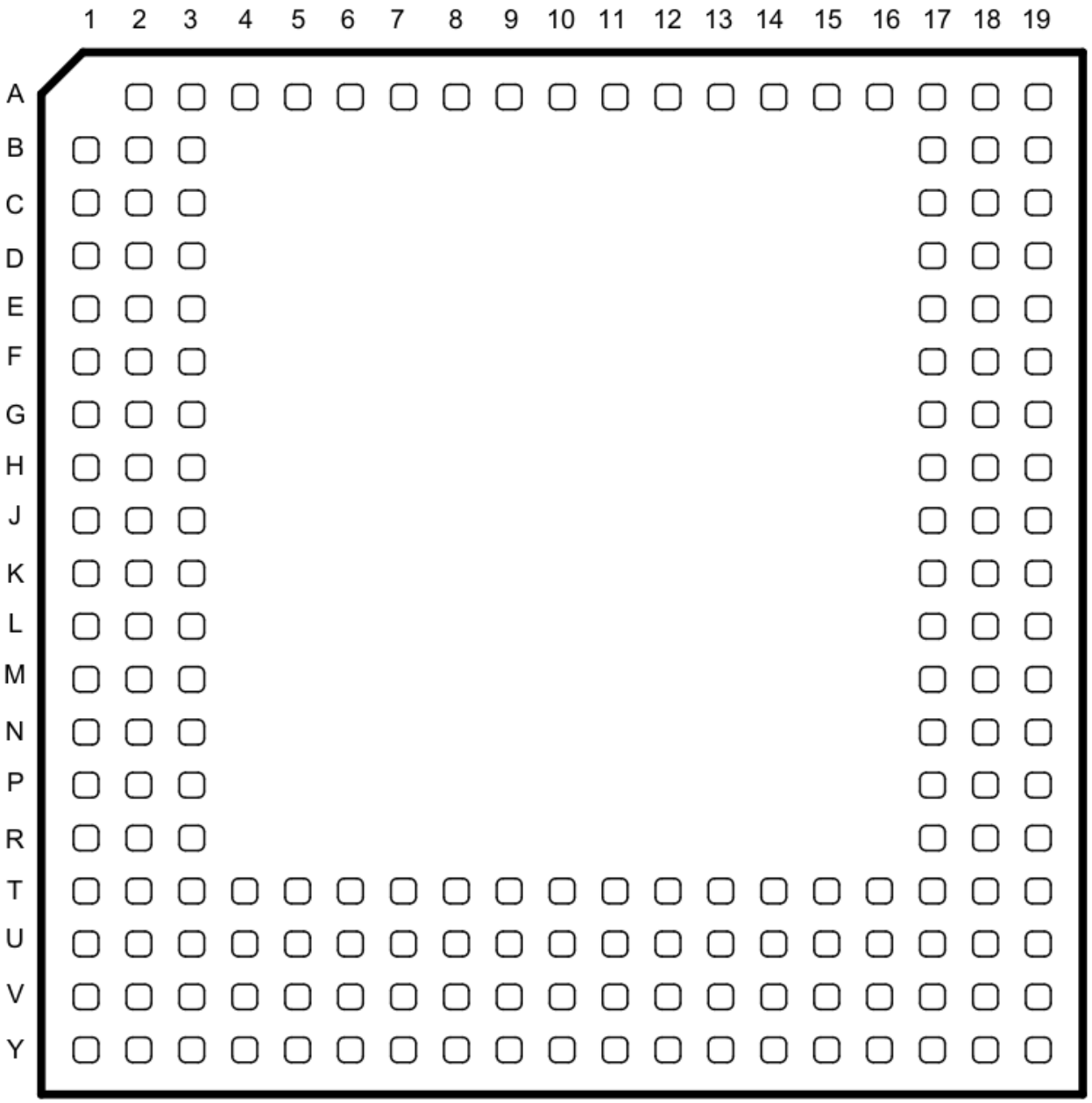


Fig. 3: Grinn AstraSOM-261x pads (top view)

5.5 Pad Description

Tab. 12: Grinn AstraSOM-261x system manager pad description

LGA Pad	MCU Ball	Name	Type	Pinmux	Domain	Delay (ps)	Note
A2	B7	GPIO32	I/O	GPIO32 / —— / RGMII_MDIO / —— / —— / —— / SPI3_SS3n / SPI4_SS3n	PWR_1V8	76.92	-
A3	B6	GPIO30	I/O	GPIO30 / —— / URT4_REn / KEY_ROW5 / SM_URT1_TXD / —— / KEY_COL5 / SPI4_SCLK	PWR_1V8	63.01	-
A4	C5	GPIO26	I/O	GPIO26 / URT5_TXD / RGMII_PTP_PPS_O / —— / SM_URT1_TXD / USB2_DRV_VBUS / —— / —— | CPU_RST_BYPASS	PWR_1V8	54.57	Should be low during reset
A5	C6	GPIO25	I/O	GPIO25 / URT5_RXD / GPIO_TRIG1 / KEY_ROW2 / SM_URT1_RXD / —— / KEY_COL1 / ——	PWR_1V8	50.52	-
A6	B2	GPIO28	I/O	GPIO28 / TW3_SDA / URT4_RXD / —— / SM_URT1_CTSn / —— / —— / ——	PWR_1V8	22.57	-
A7	B3	GPIO24	I/O	GPIO24 / TW2_SDA / RGMII_MDIO / KEY_ROW1 / —— / SPI3_SS3n / KEY_COL2 / ——	PWR_1V8	22.30	-
A8	A3	GPIO27	I/O	GPIO27 / TW3_SCL / URT4_TXD / —— / SM_URT1_RTSn / —— / —— / ——	PWR_1V8	9.39	-
A9	B4	GPIO23	I/O	GPIO23 / TW2_SCL / RGMII_MDC / KEY_ROW0 / —— / SPI3_SS2n / KEY_COL3 / ——	PWR_1V8	6.69	-
A10	A6	GPIO29	I/O	GPIO29 / —— / URT4_DE / KEY_ROW4 / SM_URT1_RXD / —— / KEY_COL4 / SPI4_SDI	PWR_1V8	7.03	-
A11	-	GND	Power	-	GND	n/a	-
A12	B16	GPIO52	I/O	GPIO52 / RGMII2_RD0 / —— / —— / —— / —— / SPI4_SS2n / SPI3_SDO	PWR_1V8	7.66	-
A13	B17	GPIO56	I/O	GPIO56 / RGMII2_RXC / —— / —— / —— / —— / —— / SPI4_SS0n	PWR_1V8	6.68	-
A14	B19	GPIO58	I/O	GPIO58 / RGMII2_TXCTL / —— / —— / —— / —— / —— / SPI4_SCLK	PWR_1V8	6.83	-
A15	B18	GPIO59	I/O	GPIO59 / RGMII2_RXCTL / —— / —— / —— / —— / —— / SPI4_SDI	PWR_1V8	18.81	-
A16	A18	GPIO57	I/O	GPIO57 / RGMII2_TXC / —— / —— / —— / —— / —— / SPI4_SDO	PWR_1V8	27.28	-
A17	A16	GPIO53	I/O	GPIO53 / RGMII2_RD1 / —— / —— / —— / —— / —— / SPI4_SS3n / SPI3_SCLK	PWR_1V8	43.78	-
A18	C19	GPIO55	I/O	GPIO55 / RGMII2_RD3 / —— / —— / —— / SPI5_SDI / —— / SPI4_SS1n	PWR_1V8	45.83	-
A19	C17	GPIO54	I/O	GPIO54 / RGMII2_RD2 / —— / —— / —— / —— / —— / SPI3_SDI	PWR_1V8	59.55	-
B1	A9	GPIO40	I/O	GPIO40 / RGMII1_RD3 / RMII2_RXD1 / KEY_ROW7 / URT6_TXD / SPI5_SS2n / SPI4_SS2n / ——	PWR_1V8	125.87	-
B2	C7	GPIO31	I/O	GPIO31 / —— / RGMII_MDC / —— / —— / SPI5_SS3n / SPI3_SS2n / SPI4_SS2n	PWR_1V8	75.20	-
B3	C8	GPIO33	I/O	GPIO33 / RGMII1_TD0 / RMII1_TXD0 / —— / —— / SM_CAN0_TX / SPI3_SS1n / SPI4_SS1n | SW_STRAP[2]	PWR_1V8	69.88	-
B17	C15	GPIO50	I/O	GPIO50 / RGMII2_TD2 / —— / —— / —— / SPI5_SCLK / —— / SPI3_SS1n	PWR_1V8	51.58	-
B18	D15	GPIO51	I/O	GPIO51 / RGMII2_TD3 / —— / —— / —— / —— / —— / SPI3_SS0n	PWR_1V8	53.40	-
B19	-	GND	Power	-	GND	n/a	-

LGA Pad	MCU Ball	Name	Type	Pinmux	Power Domain	Delay (ps)	Note
C1	D11	GPIO39	I/O	GPIO39 / RGMII1_RD2 / RMII2_RXD0 / KEY_ROW6 / URT6_RXD / SPI5_SS1n / SPI4_SS3n / ——	PWR_1V8	94.04	-
C2	-	GND	Power	-	GND	n/a	-
C3	F10	GPIO34	I/O	GPIO34 / RGMII1_TD1 / RMII1_TXD1 / —— / —— / SM_CAN0_RX / —— / ——	PWR_1V8	73.62	-
C17	G23	SM_GPIO9	I/O	SM_GPIO9 / SM_SPI1_SDO / SM_SPI1S_SDO / SM_PWM3 / —— / —— / —— / —— | BOOT_SRC[1]	PWR_1V8	25.74	-
C18	F17	GPIO49	I/O	GPIO49 / RGMII2_TD1 / —— / —— / —— / SPI5_SDO / SPI4_SS3n / SPI3_SS2n	PWR_1V8	53.16	-
C19	D22	SM_GPIO37	I/O	SM_GPIO37 / SM_PWM6 / —— / SM_TW0_SCL / KEY_ROW6 / SM_PDM_CLKIO / —— / ——	PWR_1V8	48.56	-
D1	B9	GPIO36	I/O	GPIO36 / RGMII1_TD3 / RMII2_TXD1 / —— / URT5_TXD / —— / —— / SPI4_SDO | SW_STRAP[3]	PWR_1V8	93.75	-
D2	B10	GPIO37	I/O	GPIO37 / RGMII1_RD0 / RMII1_RXD0 / —— / —— / SM_CAN1_TX / —— / SPI5_SDI	PWR_1V8	87.51	-
D3	C9	GPIO35	I/O	GPIO35 / RGMII1_TD2 / RMII2_TXD0 / KEY_COL7 / URT5_RXD / —— / —— / SPI4_SS0n	PWR_1V8	74.84	-
D17	-	GND	Power	-	GND	n/a	-
D18	F15	GPIO48	I/O	GPIO48 / RGMII2_TD0 / —— / —— / —— / SPI5_SS0n / SPI4_SS2n / SPI3_SS3n	PWR_1V8	73.37	-
D19	B21	SM_GPIO33	I/O	SM_GPIO33 / SM_PWM2 / —— / SM_URT2_TXD / SM_URT3_RTSn / KEY_ROW5 / SM_URT3_DE / ——	PWR_1V8	69.75	-
E1	B12	GPIO42	I/O	GPIO42 / RGMII1_TXC / RMII2_CRSDV / KEY_ROW8 / URT7_RXD / —— / SPI4_SCLK / ——	PWR_1V8	108.34	-
E2	B11	GPIO41	I/O	GPIO41 / RGMII1_RXC / RMII1_CRSDV / —— / —— / —— / —— / SPI5_SCLK	PWR_1V8	91.28	-
E3	C13	GPIO44	I/O	GPIO44 / RGMII1_RXCTL / RMII2_TXEN / KEY_ROW9 / URT7_TXD / —— / SPI4_SDI / ——	PWR_1V8	84.38	-
E17	T30	SM_GPIO1	I/O	SM_TDI / SM_GPIO1 / SM_URT0_RXD / KEY_COL1 / GPIO_TRIG0 / SM_PWM9 / KEY_ROW7 / ——	PWR_1V8	6.69	-
E18	F23	SM_GPIO10	I/O	SM_GPIO10 / SM_SPI1_SCLK / SM_SPI1S_SCLK / SM_PWM4 / —— / —— / —— / ——	PWR_1V8	52.01	-
E19	D24	SM_GPIO11	I/O	SM_GPIO11 / SM_SPI1_SDI / SM_SPI1S_SDI / SM_PWM5 / —— / —— / —— / ——	PWR_1V8	51.80	-
F1	A13	GPIO45	I/O	GPIO45 / RGMII1_CLKOUT / RMII1_REFCLK / —— / ——- / —— / —— / ——	PWR_1V8	116.56	-
F2	B13	GPIO43	I/O	GPIO43 / RGMII1_TXCTL / RMII1_TXEN / —— / —— / —— / SPI4_SS0n / —— | SW_STRAP[0]	PWR_1V8	105.86	Pull-down 2.2 kΩ
F3	-	GND	Power	-	GND	n/a	-
F17	V30	SM_GPIO0	I/O	SM_TMS / SM_GPIO0 / SM_URT0_TXD / KEY_COL0 / —— / SM_PDM_DI0 / SM_PWM10 / ——	PWR_1V8	6.77	-
F18	V31	POR_EN	Input	SM_POR_EN	PWR_1V8	7.05	-
F19	B25	SM_GPIO6	I/O	SM_GPIO6 / SM_SPI1_SS3n / SM_SPI1S_SSn / SM_PWM2 / —— / —— / —— / ——	PWR_1V8	57.54	-
G1	-	GND	Power	-	GND	n/a	-

LGA Pad	MCU Ball	Name	Type	Pinmux	Power Domain	Delay (ps)	Note
G2	-	GND	Power	-	GND	n/a	-
G3	F13	GPIO38	I/O	GPIO38 / RGMII1_RD1 / RMII1_RXD1 / —— / —— / SM_CAN1_RX / —— / SPI5_SDO	PWR_1V8	87.03	-
G17	AA29	GPIO1	I/O	GPIO1 / I2S1_BCLK / —— / —— / —— / —— / —— / SPI3_SCLK	PWR_1V8	6.76	-
G18	AA31	GPIO0	I/O	GPIO0 / I2S1_LRCK / —— / —— / —— / —— / —— / SPI3_SS0n	PWR_1V8	7.31	-
G19	W29	GPIO3	I/O	GPIO3 / I2S1_MCLK / —— / —— / —— / —— / —— / SPI3_SS1n	PWR_1V8	21.70	-
H1	AD2	USB2_1_D_P	Interface	USB2_1_Dp	PWR_1V8	146.91	-
H2	AC2	USB2_1_D_N	Interface	USB2_1_Dn	PWR_1V8	146.98	-
H3	AC1	USB2_1_VBUS	Interface	USB2_1_VBUS	PWR_1V8	89.92	30 kΩ series resistor
H17	AA30	GPIO2	I/O	GPIO2 / I2S1_DO / —— / —— / SPDIFO / —— / —— / SPI3_SDO	PWR_1V8	8.98	-
H18	AB30	GPIO4	I/O	GPIO4 / I2S1_DI / —— / —— / SPDIFI / —— / —— / SPI3_SDI	PWR_1V8	25.59	-
H19	-	GND	Power	-	GND	n/a	-
J1	AF2	USB2_0_D_P	Interface	USB2_0_Dp	PWR_1V8	116.33	-
J2	AE2	USB2_0_D_N	Interface	USB2_0_Dn	PWR_1V8	116.07	-
J3	AH2	USB2_0_ID	Interface	USB2_0_ID	PWR_1V8	89.13	-
J17	U30	SM_GPIO2	I/O	SM_TDO / SM_GPIO2 / SM_PDM_CLKIO / I2S2_MCLK / —— / —— / SM_PWM11 / ——	PWR_1V8	33.68	-
J18	W30	TCK	Debug	SM_TCK	PWR_1V8	26.75	-
J19	B22	SM_GPIO38	I/O	SM_GPIO38 / SM_PWM7 / —— / SM_TW0_SDA / —— / SM_PDM_DI0 / —— / ——	PWR_1V8	110.95	-
K1	-	GND	Power	-	GND	n/a	-
K2	-	GND	Power	-	GND	n/a	-
K3	AH3	USB2_0_VBUS	Interface	USB2_0_VBUS	PWR_1V8	99.59	30 kΩ series resistor
K17	AF28	GPIO22	I/O	GPIO22 / SPI2_SDI / —— / SDIO2_CDn / SDIO1_CDn / —— / —— / ——	PWR_1V8	23.98	-
K18	AG29	GPIO18	I/O	GPIO18 / SPI2_SS2n / CAM_DATA6 / SDIO2_DAT1 / PDM_DI2 / SM_CAN1_RX / —— / ——	PWR_1V8	52.05	-
K19	AG30	GPIO16	I/O	GPIO16 / SPI2_SS0n / —— / SDIO2_DAT3 / —— / —— / —— / ——	PWR_1V8	32.58	-
L1	U26	SM_GPIO8	I/O	SM_GPIO8 / SM_URT0_TXD / SM_CAN0_TX / SM_CLKOUT / —— / —— / SM_URT1_TXD / —— | BOOT_SRC[0]	PWR_1V8	200.10	UART CLI TX
L2	AA25	GPIO8	I/O	GPIO8 / I2S2_DI / CAM_VSYNC / KEY_ROW3 / SPDIFI / —— / KEY_COL4 / ——	PWR_1V8	167.07	-
L3	F19	SM_GPIO31	I/O	SM_GPIO31 / SM_PWM0 / SM_URT1_RXD / KEY_ROW7 / SM_PDM_DI0 / SM_URT0_RXD / SM_CAN1_RX / ——	PWR_1V8	190.77	-
L17	H30	SM_GPIO29	I/O	SM_GPIO29 / SM_XSPI_DATA6 / SM_URT3_RXD / KEY_COL5 / SM_URT2_CTSn / SM_URT0_CTSn / KEY_ROW2 / SM_URT1_CTSn	PWR_1V8	91.23	-
L18	AG28	GPIO17	I/O	GPIO17 / SPI2_SS1n / CAM_DATA5 / SDIO2_DAT2 / —— / DSI_TE / —— / ——	PWR_1V8	41.32	-
L19	AF31	GPIO19	I/O	GPIO19 / SPI2_SS3n / CAM_DATA7 / SDIO2_DAT0 / PDM_DI3 / SM_CAN1_TX / —— / ——	PWR_1V8	26.02	-

LGA Pad	MCU Ball	Name	Type	Pinmux	Power Domain	Delay (ps)	Note
M1	T29	AUDIO_MUTE	Input	SM_AUDIO_MUTE	PWR_1V8	197.20	-
M2	AA26	GPIO7	I/O	GPIO7 / I2S2_DO / —— / KEY_ROW2 / SPDIFO / SM_PDM_CLKIO / KEY_ROW5 / ——	PWR_1V8	175.14	-
M3	P29	SM_GPIO14	I/O	SM_GPIO14 / SM_TW1_SCL / SM_URT0_CTSn / SM_PWM10 / SM_CAN0_RX / —— / SM_URT1_CTSn / ——	PWR_1V8	186.18	-
M17	J29	SM_GPIO28	I/O	SM_GPIO28 / SM_XSPI_DATA5 / SM_URT3_TXD / KEY_COL4 / SM_URT2_RTSn / SM_URT0_RTSn / KEY_ROW3 / SM_URT1_RTSn	PWR_1V8	82.54	-
M18	AF27	GPIO21	I/O	GPIO21 / SPI2_SCLK / —— / SDIO2_CLK / —— / CLKOUT / —— / —— | SW_STRAP[1]	PWR_1V8	78.51	Pull-up 2.2 kΩ depending on ram configuration
M19	AH28	GPIO20	I/O	GPIO20 / SPI2_SDO / —— / SDIO2_CMD / —— / —— / —— / ——	PWR_1V8	39.70	-
N1	AC31	GPIO5	I/O	GPIO5 / I2S2_LRCK / CAM_PIXCLK / KEY_ROW0 / SPDIFI / —— / KEY_ROW7 / ——	PWR_1V8	191.21	-
N2	-	GND	Power	-	GND	n/a	-
N3	F21	SM_GPIO35	I/O	SM_GPIO35 / SM_PWM4 / SM_URT1_RTSn / SM_URT3_TXD / SM_URT2_RTSn / KEY_ROW3 / SM_URT0_RTSn / ——	PWR_1V8	180.99	-
N17	P28	SM_GPIO18	I/O	SM_GPIO18 / SM_XSPI_CS0n / —— / —— / —— / —— / —— / ——	PWR_1V8	74.19	-
N18	K29	SM_GPIO27	I/O	SM_GPIO27 / SM_XSPI_DATA4 / SM_URT2_RXD / KEY_COL3 / SM_UART3_CTSn / SM_URT3_REn / KEY_ROW4 / ——	PWR_1V8	92.79	-
N19	M29	SM_GPIO24	I/O	SM_GPIO24 / SM_XSPI_CLKn / —— / —— / —— / —— / —— / ——	PWR_1V8	101.25	-
P1	AC30	GPIO6	I/O	GPIO6 / I2S2_BCLK / CAM_HSYNC / KEY_ROW1 / SPDIFO / —— / KEY_ROW6 / ——	PWR_1V8	174.56	-
P2	W25	CAM-ERA_MUTE	Input	CAMERA_MUTE	PWR_1V8	154.56	-
P3	W26	TRSTn	Debug	SM_TRSTn	PWR_1V8	148.35	-
P17	-	GND	Power	-	GND	n/a	-
P18	P26	SM_GPIO25	I/O	SM_GPIO25 / SM_XSPI_DQS / —— / —— / —— / —— / KEY_ROW6 / ——	PWR_1V8	94.77	-
P19	M27	SM_GPIO23	I/O	SM_GPIO23 / SM_XSPI_CLK / —— / —— / —— / —— / —— / ——	PWR_1V8	102.49	-
R1	AD30	GPIO11	I/O	GPIO11 / I2S2_MCLK / CAM_DATA2 / —— / SM_PDM_CLKIO / —— / —— / ——	PWR_1V8	173.37	-
R2	T31	SM_GPIO7	I/O	SM_GPIO7 / SM_URT0_RXD / SM_CAN0_RX / KEY_ROW6 / GPIO_TRIG2 / SM_PWM9 / SM_URT1_RXD / ——	PWR_1V8	179.25	UART CLI RX
R3	-	GND	Power	-	GND	n/a	-
R17	H29	SM_GPIO30	I/O	SM_GPIO30 / SM_XSPI_DATA7 / —— / KEY_COL6 / —— / —— / —— / SM_CLKOUT	PWR_1V8	119.08	-
R18	L29	SM_GPIO26	I/O	SM_GPIO26 / SM_XSPI_CS1n / SM_URT2_TXD / KEY_COL2 / SM_URT3_RTSn / SM_URT3_DE / KEY_ROW5 / SM_CLKOUT	PWR_1V8	115.94	-
R19	M30	SM_GPIO20	I/O	SM_GPIO20 / SM_XSPI_DATA1 / —— / —— / —— / —— / —— / ——	PWR_1V8	127.68	-

LGA Pad	MCU Ball	Name	Type	Pinmux	Power Domain	Delay (ps)	Note
T1	C14	GPIO46	I/O	GPIO46 / SDIO1_CDn / SDIO2_CDn / KEY_COL0 / ———- / SM_URT1_RSTn / KEY_ROW9 / DSI_TE	PWR_1V8	213.21	-
T2	B14	GPIO47	I/O	GPIO47 / SDIO1_WP / SDIO2_WP / KEY_COL1 / RMII2_REFCLK / SM_URT1_CSTn / KEY_ROW8 / ———	PWR_1V8	237.51	-
T3	-	GND	Power	-	GND	n/a	-
T4	A24	SM_GPIO4	I/O	SM_TW1_SDA	PWR_1V8	268.43	Pull-up 2.2 kΩ
T5	R29	STANDBY_EN	Output	SM_GPIO16	PWR_1V8	221.73	Pull-down 200 kΩ
T6	-	GND	Power	-	GND	n/a	-
T7	A21	SM_GPIO32	I/O	SM_GPIO32 / SM_PWM1 / SM_URT1_TXD / KEY_COL0 / SM_PDM_CLKIO / SM_URT0_TXD / SM_CAN1_TX / ———	PWR_1V8	241.17	-
T8	-	GND	Power	-	GND	n/a	-
T9	AG13	SDIO_DATA1	Interface	SDIO_DATA1	PWR_1V8_CTL	138.54	-
T10	AH13	SDIO_DATA2	Interface	SDIO_DATA2	PWR_1V8_CTL	123.66	-
T11	AF12	SDIO_CLK	Interface	SDIO_CLK	PWR_1V8_CTL	104.97	-
T12	A28	SM_ADCI2	Analog	SM_ADCI2	PWR_1V8	178.10	-
T13	AC27	GPIO13	I/O	GPIO13 / I2S3_BCLK / PDM_DI1 / RGMII_PTP_PPS_0 / USB2_DRV_VBUS / ——— / ——— / ———	PWR_1V8	126.63	-
T14	AE24	GPIO12	I/O	GPIO12 / I2S3_LRCK / CAM_DATA3 / SDIO2_WP / SDIO1_WP / ——— / ——— / ———	PWR_1V8	98.45	-
T15	C30	SM_ADCI6	Analog	SM_ADCI6	PWR_1V8	192.21	-
T16	B30	SM_ADCI5	Analog	SM_ADCI5	PWR_1V8	186.32	-
T17	N31	SM_GPIO19	I/O	SM_GPIO19 / SM_XSPI_DATA0 / ——— / ——— / ——— / ——— / ——— / ———	PWR_1V8	120.72	-
T18	L31	SM_GPIO21	I/O	SM_GPIO21 / SM_XSPI_DATA2 / ——— / ——— / ——— / ——— / ——— / ———	PWR_1V8	129.90	-
T19	L30	SM_GPIO22	I/O	SM_GPIO22 / SM_XSPI_DATA3 / ——— / ——— / ——— / ——— / ——— / ———	PWR_1V8	140.20	-
U1	-	GND	Power	-	GND	n/a	-
U2	-	GND	Power	-	GND	n/a	-
U3	-	GND	Power	-	GND	n/a	-
U4	C24	SM_GPIO3	I/O	SM_TW1_SCL	PWR_1V8	261.29	Pull-up 2.2 kΩ
U5	U25	SM_GPIO13	I/O	SM_GPIO13 / SM_TW0_SDA / SM_I3C_MS_SDA / SM_CLKOUT / ——— / ——— / ——— / ———	PWR_1V8	210.20	-
U6	C21	SM_GPIO34	I/O	SM_GPIO34 / SM_PWM3 / ——— / SM_URT2_RXD / SM_URT3_CTSn / KEY_ROW4 / SM_URT3_REn / ———	PWR_1V8	254.97	-
U7	-	GND	Power	-	GND	n/a	-
U8	-	GND	Power	-	GND	n/a	-
U9	AF13	SDIO_DATA3	Interface	SDIO_DATA3	PWR_1V8_CTL	141.59	-
U10	AG12	SDIO_CMD	Interface	SDIO_CMD	PWR_1V8_CTL	145.53	-
U11	AF14	SDIO_DATA0	Interface	SDIO_DATA0	PWR_1V8_CTL	125.58	-
U12	C22	SM_GPIO36	I/O	SM_GPIO36 / SM_PWM5 / SM_URT1_CTSn / SM_URT3_RXD / SM_URT2_CTSn / KEY_ROW2 / SM_URT0_CTSn / ———	PWR_1V8	201.30	-
U13	AF30	GPIO14	I/O	GPIO14 / I2S3_DO / ——— / ——— / PDM_DI3 / ——— / SPDIFO / ———	PWR_1V8	119.97	-
U14	AC25	GPIO15	I/O	GPIO15 / I2S3_DI / CAM_DATA4 / ——— / SM_PDM_DI0 / ——— / SPDIFI / ———	PWR_1V8	105.67	-

LGA Pad	MCU Ball	Name	Type	Pinmux	Power Domain	Delay (ps)	Note
U15	P30	SM_GPIO15	I/O	SM_GPIO15 / SM_TW1_SDA / SM_URT0_RTSn / SM_PWM11 / SM_CAN0_TX / —— / SM_URT1_RTSn / ——	PWR_1V8	144.90	-
U16	B28	SM_ADCI3	Analog	SM_ADCI3	PWR_1V8	191.94	-
U17	AB28	GPIO9	I/O	GPIO9 / —— / CAM_DATA0 / —— / PDM_DI1 / —— / —— / ——	PWR_1V8	94.38	-
U18	-	GND	Power	-	GND	n/a	-
U19	-	GND	Power	-	GND	n/a	-
V1	-	VSYS	Power Input	-	VSYS	n/a	-
V2	-	VSYS	Power Input	-	VSYS	n/a	-
V3	-	GND	Power	-	GND	n/a	-
V4	-	PWR_3V3	Power Output	-	PWR_3V3	n/a	-
V5	U28	SM_GPIO12	I/O	SM_GPIO12 / SM_TW0_SCL / SM_I3C_MS_SCL / SM_PWM6 / —— / —— / —— / ——	PWR_1V8	207.44	-
V6	-	PWR_1V8_CTL	Power Output	-	PWR_1V8_CTL	n/a	-
V7	-	GND	Power	-	GND	n/a	-
V8	AG15	CSI_D1_P	Interface	MIPI_CSI_D1p	PWR_1V8	103.70	-
V9	AH17	CSI_D0_P	Interface	MIPI_CSI_D0p	PWR_1V8	104.34	-
V10	-	GND	Power	-	GND	n/a	-
V11	AH19	CSI_CK_P	Interface	MIPI_CSI_CKp	PWR_1V8	117.79	-
V12	AG20	DSI_D3_P	Interface	MIPI_DSI_D3p	PWR_1V8	137.68	-
V13	-	GND	Power	-	GND	n/a	-
V14	AG22	DSI_D2_P	Interface	MIPI_DSI_D2p	PWR_1V8	102.42	-
V15	AF23	DSI_CK_P	Interface	MIPI_DSI_CKp	PWR_1V8	110.88	-
V16	-	GND	Power	-	GND	n/a	-
V17	AH24	DSI_D1_P	Interface	MIPI_DSI_D1p	PWR_1V8	95.67	-
V18	AG26	DSI_D0_P	Interface	MIPI_DSI_D0p	PWR_1V8	99.57	-
V19	-	GND	Power	-	GND	n/a	-
Y1	-	VSYS	Power Input	-	VSYS	n/a	-
Y2	-	VSYS	Power Input	-	VSYS	n/a	-
Y3	-	GND	Power	-	GND	n/a	-
Y4	-	PWR_1V8	Power Output	-	PWR_1V8	n/a	-
Y5	AE30	GPIO10	I/O	GPIO10 / —— / CAM_DATA1 / —— / PDM_DI2 / DSI_TE / —— / ——	PWR_1V8	201.19	-
Y6	U29	SM_RSTn	Output	SM_RSTn	PWR_1V8	220.61	Pull-up 2.2 kΩ, capacitor 100nF
Y7	-	PWR_3V3_CTL	Power Output	-	PWR_3V3_CTL	n/a	-
Y8	AG16	CSI_D1_N	Interface	MIPI_CSI_D1n	PWR_1V8	103.83	-
Y9	AG17	CSI_D0_N	Interface	MIPI_CSI_D0n	PWR_1V8	104.11	-
Y10	-	GND	Power	-	GND	n/a	-
Y11	AG19	CSI_CK_N	Interface	MIPI_CSI_CKn	PWR_1V8	118.05	-
Y12	AG21	DSI_D3_N	Interface	MIPI_DSI_D3n	PWR_1V8	137.28	-
Y13	-	GND	Power	-	GND	n/a	-
Y14	AH22	DSI_D2_N	Interface	MIPI_DSI_D2n	PWR_1V8	102.81	-
Y15	AF24	DSI_CK_N	Interface	MIPI_DSI_CKn	PWR_1V8	110.42	-
Y16	-	GND	Power	-	GND	n/a	-
Y17	AG24	DSI_D1_N	Interface	MIPI_DSI_D1n	PWR_1V8	95.64	-
Y18	AH26	DSI_D0_N	Interface	MIPI_DSI_D0n	PWR_1V8	99.50	-

LGA Pad	MCU Ball	Name	Type	Pinmux	Power Domain	Delay (ps)	Note
Y19	-	GND	Power	-	GND	n/a	-

Note

- **SM_ADC1/7/4/0** are not available at LGA and connected to ground on SOM.
- Pins **SM_GPIO3** and **SM_GPIO4** must be configured as **SM_TW1**.
- I2C Address `0x60` is reserved on **SM_TW1**.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

	Maximum	Unit
Supply voltage **VSYS**	5.5	V

6.2 Recommended Operating Conditions

Tab. 13: Operating conditions

	Minimum	Nominal	Maximum	Unit
Supply voltage **VSYS**[1]	3.2	5.0	5.5	V
Ambient operating temperature (commercial grade)	0	—	70	°C
Ambient operating temperature (industrial grade)	-40	—	85	°C

[1] For VSYS voltage between 3.20V and 3.80V, no external **PWR_3V3** and **PWR_3V3_CTL** load is allowed.

7 Mechanical Characteristics

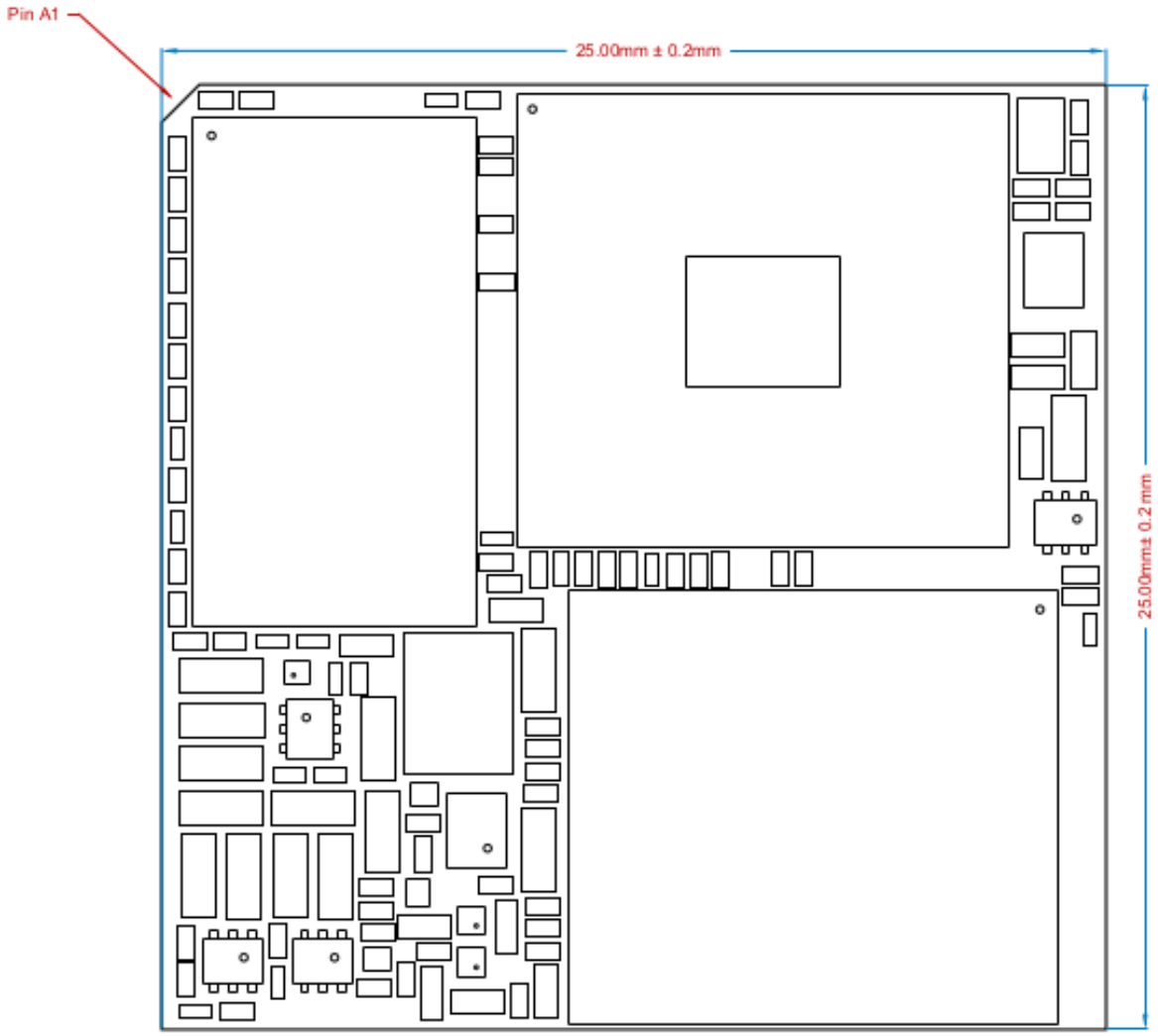


Fig. 4: Grinn AstraSOM-261x top view

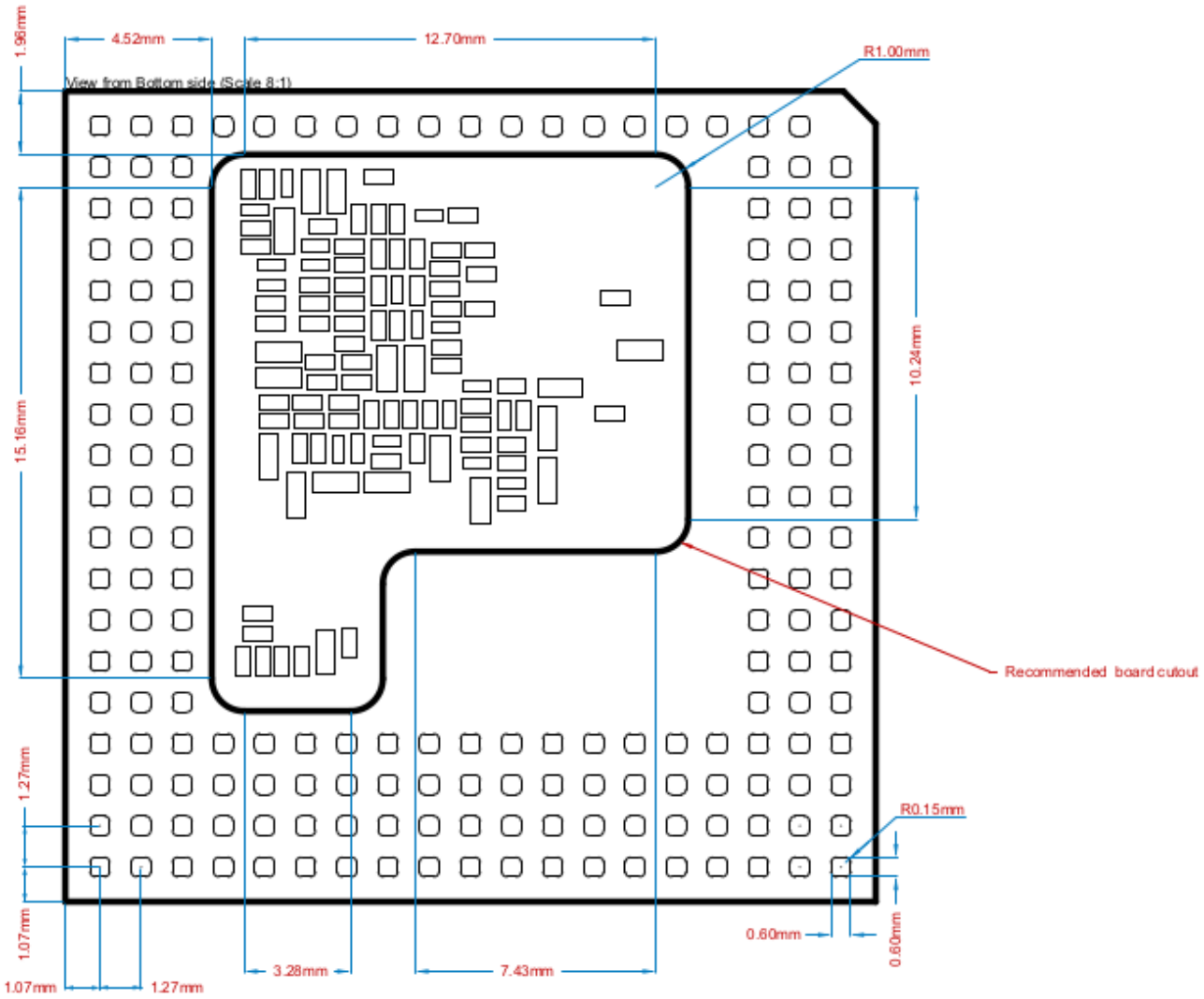
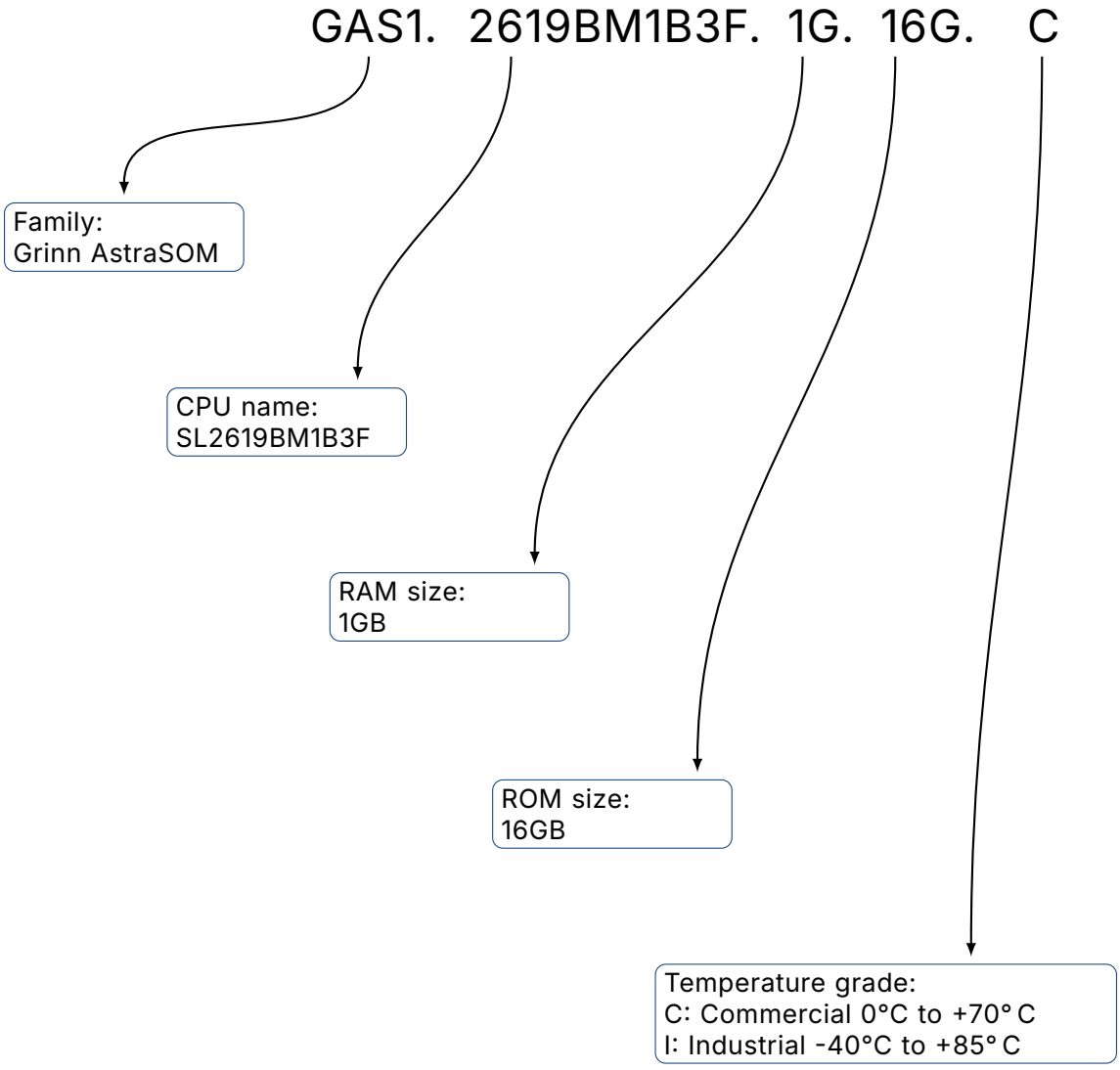
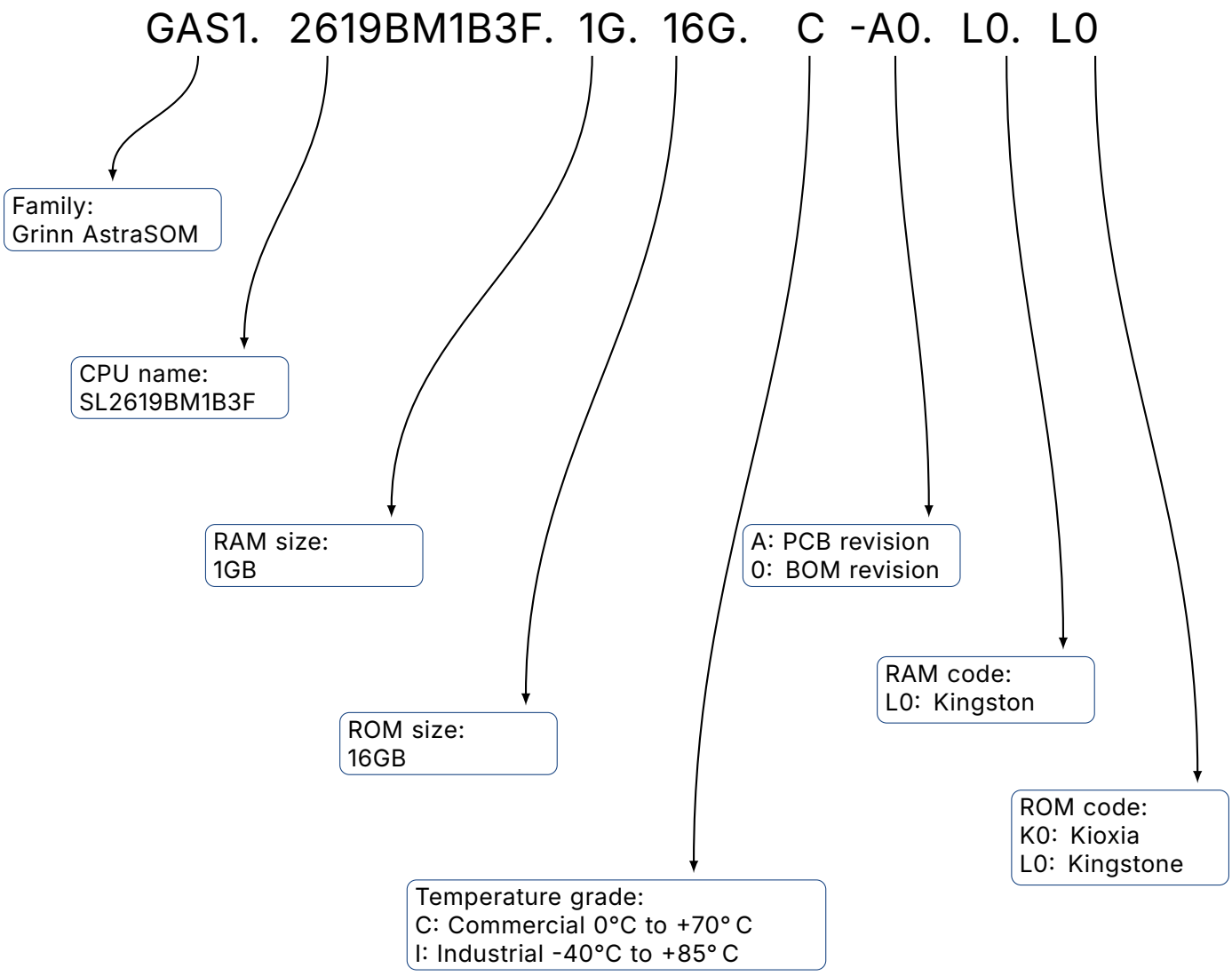


Fig. 5: Grinn AstraSOM-261x bottom view

8 Ordering Part Number



9 Full Part Number



9.1 Detailed Information on RAM Codes

Tab. 14: Detailed RAM code information.

Code	Manufacturer	Part Number
L0	Kingston	D5116AN9CXGXN-UF

9.2 Detailed Information on ROM Codes

Tab. 15: Detailed ROM code information.

Code	Manufacturer	Part Number
K0	Kioxia	THGAMVG7T13BAIL
L0	Kingston	EMMC16G-MW28-03010

Revision History

Revision	Date	Description
1.0	2026-03-20	Initial release.
1.1	2026-04-14	Change in part ordering, minor visual changes.

Grinn sp. z o.o.

Strzegomska 140a
54-429 Wrocław, Poland

grinn-global.com
office@grinn-global.com
+48 71 716 40 99