GRINN

Datasheet

Grinn AstraTwoSBC-261x

Developer Portal | Prebuilt Firmware | Code Repository | Support Page

1 Features

- A carrier board solution for AstraSOM-261x modules
- Pico-ITX form factor
- 12–24 V DC input and PoE input path
- 2x Gigabit Ethernet interfaces with onboard PHYs
- 1x USB-C 2.0 device/debug connector
- 2x USB-A 2.0 host connectors
- 1x CAN interface with onboard TCAN1044V transceiver
- 1x M.2 Key E connector for Wi-Fi/Bluetooth modules
- 1x 2-lane MIPI CSI-2 camera connector
- 1x 4-lane MIPI DSI display connector
- 1x 40-pin Raspberry Pi-style expansion header
- Cortex JTAG connector, boot/reset controls, user button, and status LEDs
- Infineon OPTIGA Trust M security controller

2 Applications

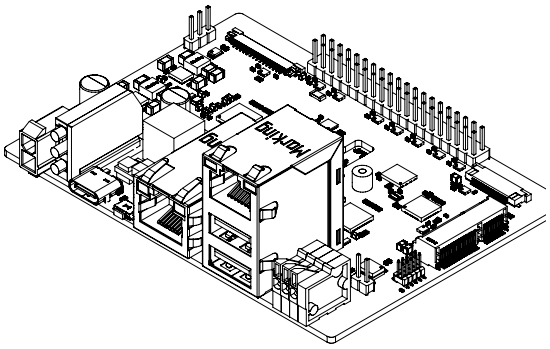
- Industrial IoT gateways
- AI-enabled edge devices
- Machine vision controllers
- Robotics and autonomous systems
- Networked control and monitoring equipment

3 Description

Grinn AstraTwoSBC-261x is a single board computer built around the Grinn AstraSOM-261x platform. The board is in the Pico-ITX format and exposes the camera, display, networking, USB, wireless, GPIO, CAN, debug, and security interfaces required for embedded Linux development and product prototyping.

The board power architecture accepts a 12–24 V DC input through the main power connector and includes a PoE input path. Onboard converters generate the 5 V and 3.3 V rails used by the SOM, external connectors, and expansion interfaces.

Expansion is provided through a 40-pin Raspberry Pi-style header, an M.2 Key E connector for wireless modules, MIPI CSI and DSI FPC connectors, USB 2.0 ports, CAN, and two Gigabit Ethernet interfaces.



Contents

4 Functional Description

4.1 Power Supply

Grinn AstraTwoSBC-261x is powered from the main 12–24 V DC input on **J2**. A PoE input path based on the **AG9912-MTB** module is connected through active OR-ing circuitry before the main buck converters.

The power tree generates the main 5 V and 3.3 V rails used by the SOM and board-level peripherals. The rail budget provides up to 5.5 A on the 5 V rail and up to 4 A on the 3.3 V rail.

Important

The PoE input requires a 48 V-class source. A PoE source providing only 24 V will not power the board through the PoE input. The PoE input path provides a 12 V, 1 A power budget and cannot supply all board loads at their indicated maximum loads simultaneously. Use the main 12–24 V DC input on **J2** when the full board power budget is required.

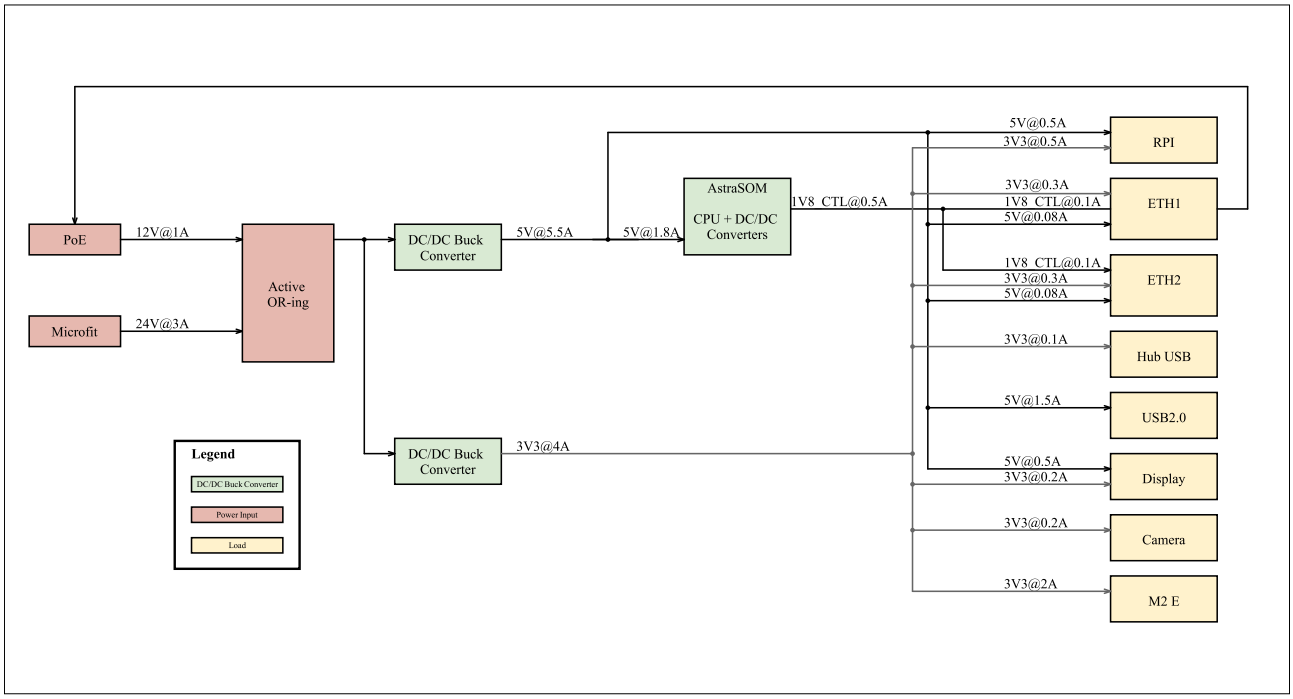


Fig. 1: Grinn AstraTwoSBC-261x power distribution block diagram.

4.2 External Cabling Recommendations

External cable selection has a direct impact on the overall EMC performance of the system. To improve robustness during immunity testing and in typical integration scenarios, the use of appropriately selected cable types and lengths is recommended for all external interfaces connected to the Grinn AstraTwoSBC-261x.

For DC power, USB-C and USB-A cable lengths should not exceed 3 m. For Ethernet connectivity, the cable length should not exceed 30 m, and shielded Ethernet cabling shall be used.

4.3 Ethernet

The board routes two RGMII Ethernet interfaces from the SOM through Microchip **KSZ9031** Gigabit Ethernet PHYs:

- **ETH1**: **RGMII1** routed through the first PHY to RJ45 connector **J5**. The connector exposes the PoE input pins **PoE_V1**...**PoE_V4**.
- **ETH2**: **RGMII2** routed through the second PHY to RJ45 plus dual USB-A connector assembly **J4**.

SOM variants based on processors other than SL2619 do not support the second RGMII interface. Verify the installed Grinn AstraSOM-261x variant before relying on **ETH2**.

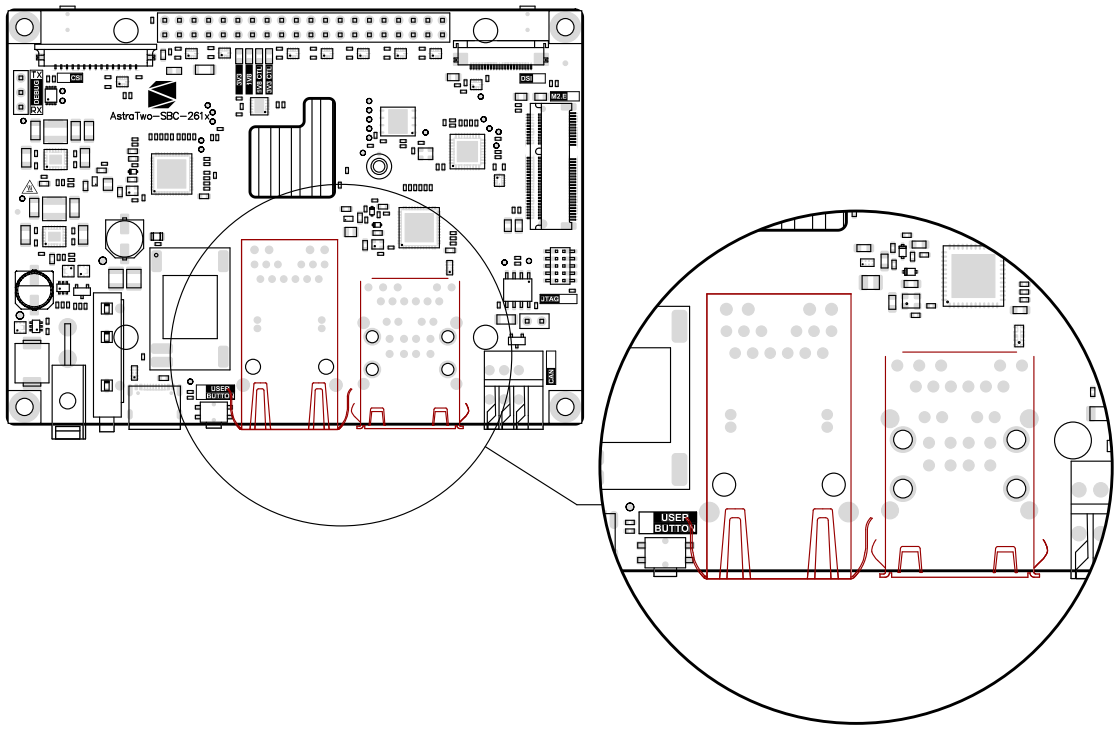


Fig. 2: Grinn AstraTwoSBC-261x Ethernet connector locations.

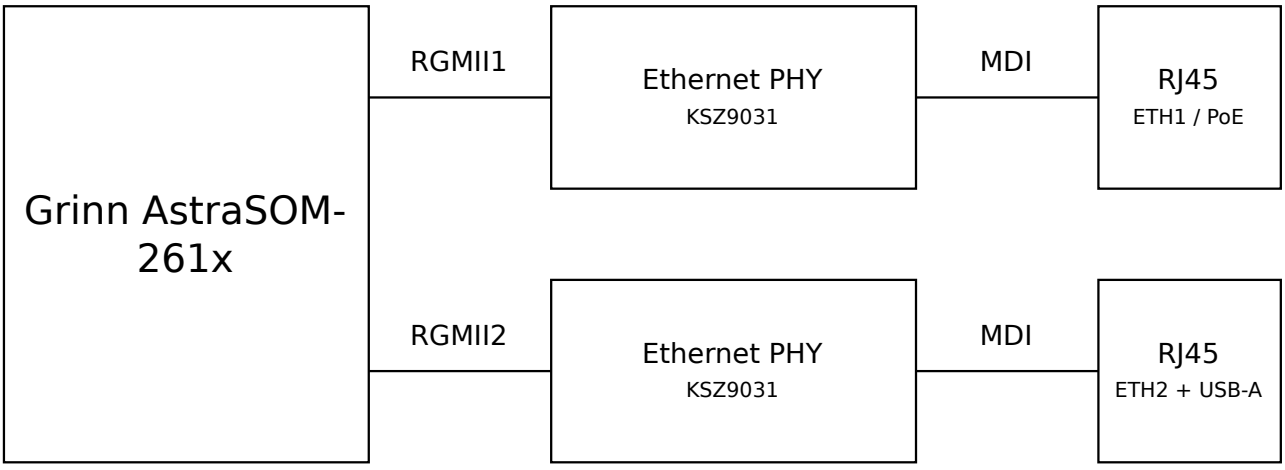


Fig. 3: Grinn AstraTwoSBC-261x Ethernet block diagram.

4.4 USB Architecture

The board includes a USB-C 2.0 device/debug connector **J3** and a USB 2.0 hub. The hub controller is **USB2513BI-AEZG**. The USB-C port is routed to the SOM USB 2.0 device interface using **DEBUG_USB_P/DEBUG_USB_N** and includes **DEBUG_VBUS** sensing.

The hub provides three downstream USB 2.0 paths with separate power-enable and overcurrent signals:

- **USB_DN0**: routed to one external USB-A connector in **J4**.
- **USB_DN1**: routed to the second external USB-A connector in **J4**.
- **USB_DN2**: routed to the M.2 Key E connector.

The two external USB-A ports use **TPS25221** load switches. Each path is current-limited to 690 mA.

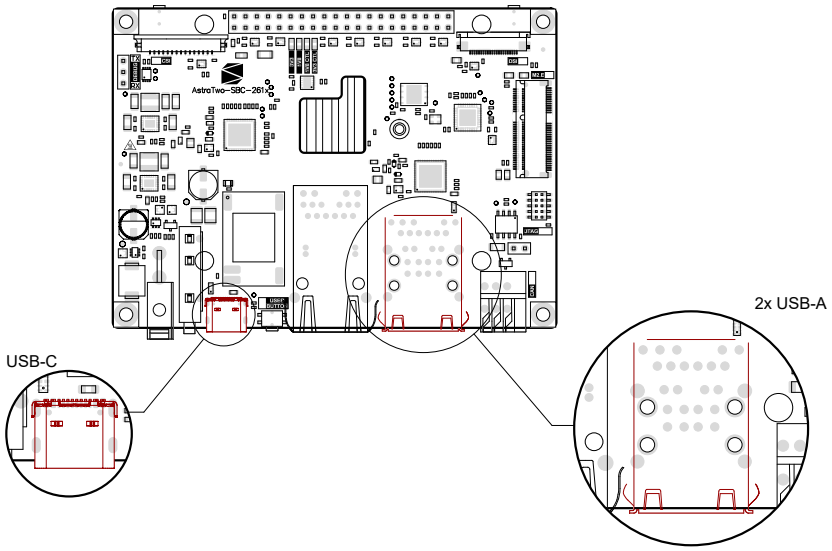


Fig. 4: Grinn AstraTwoSBC-261x USB connector locations.

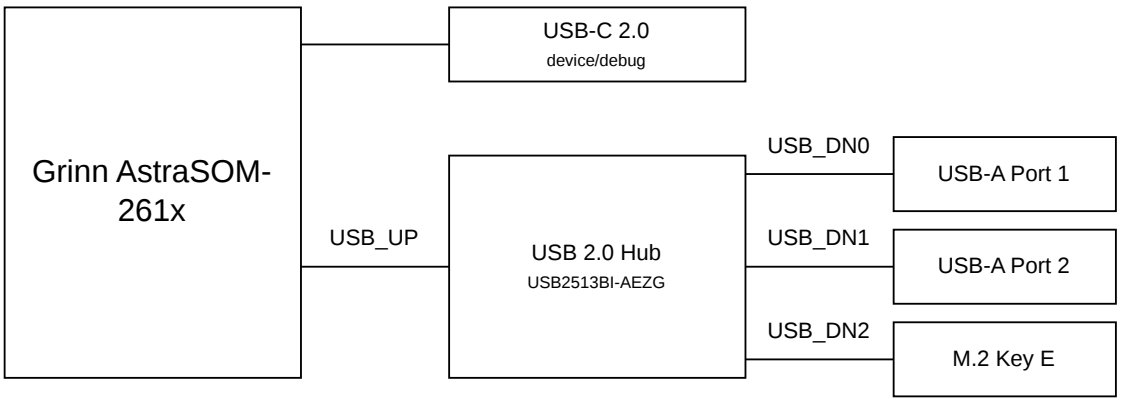


Fig. 5: Grinn AstraTwoSBC-261x USB architecture block diagram.

4.4.1 USB-C Port

The USB-C connector on the Grinn AstraTwoSBC-261x is used for ADB (Android Debug Bridge) communication. When connected to a host PC, it enumerates as an ADB device and provides access to the Android shell and development tools. The connector is also used as the USB device connection to the host PC when flashing the system image; see Section 5.4.

4.5 M.2 Key E

The **U_M2_E** block is intended for Wi-Fi and Bluetooth modules. The M.2 Key E connector is marked as **J1** and uses the 3.3 V rail for module power. The connector carries USB 2.0, UART, SDIO, I²C, suspend clock, wake, reset, and disable signals.

The **TCA9537DGSR** I/O expander is connected to **MIPI_I2C/TW3** (**i2c3** in Linux) through **M2_SCL** and **M2_SDA**; its 7-bit I²C address is 0x48. Pins P0–P2 route to M.2 vendor-defined pins 38, 40, and 42, P3 routes to **ALERTn**, and **INTn** routes to **M2_INT_EXP**.

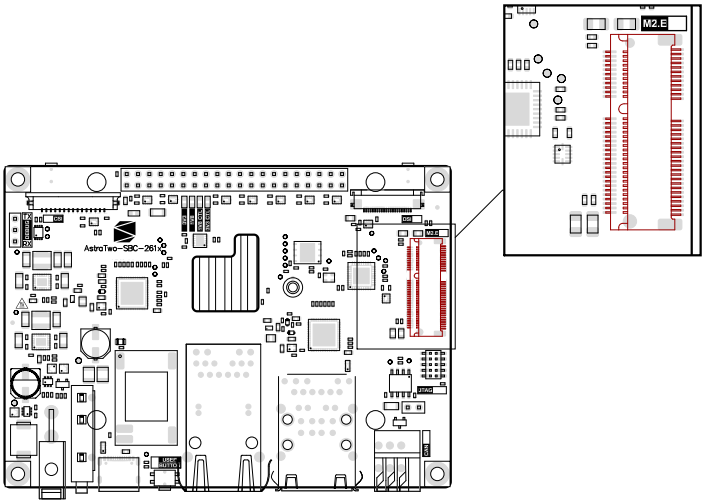


Fig. 6: Grinn AstraTwoSBC-261x M.2 Key E connector location.

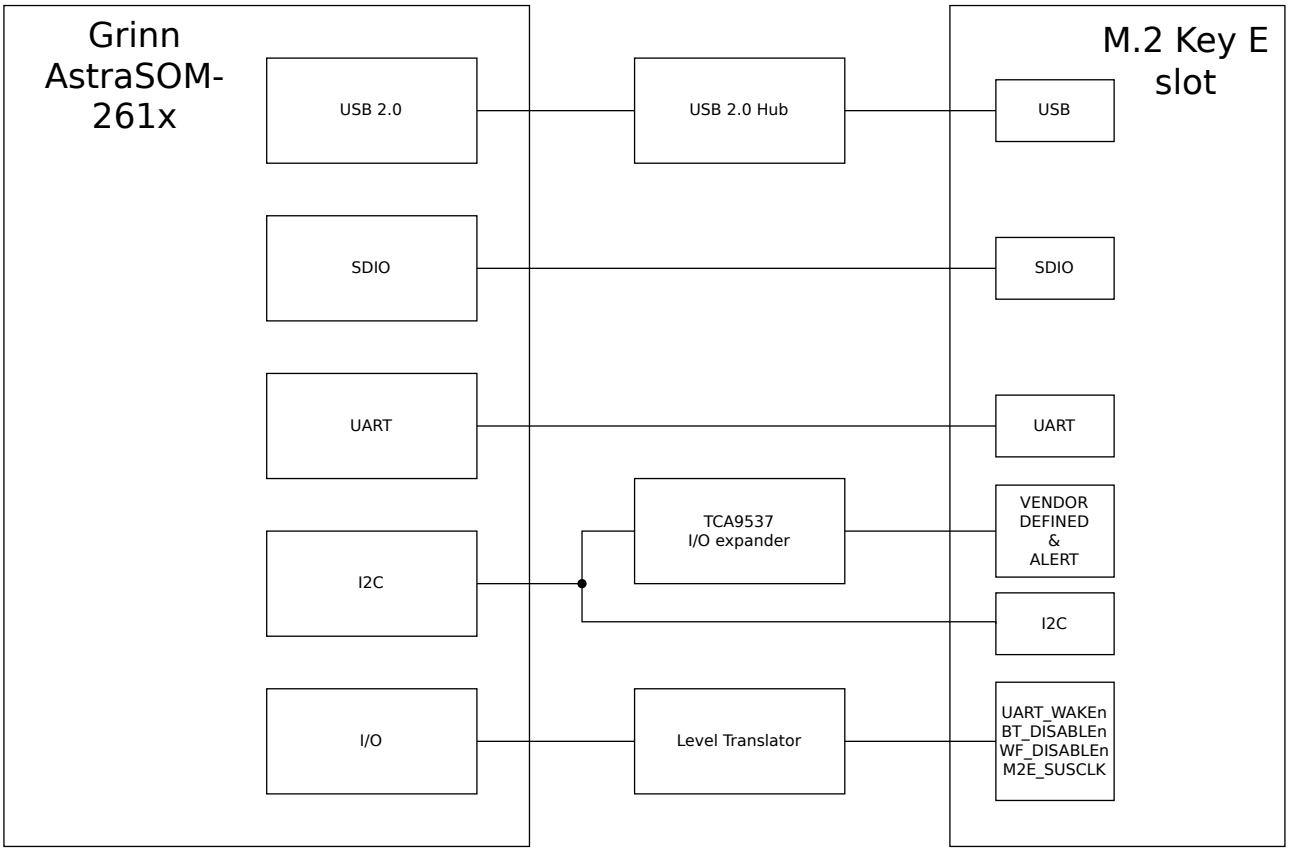


Fig. 7: Grinn AstraTwoSBC-261x M.2 Key E interface block diagram.

Tab. 1: Grinn AstraTwoSBC-261x M.2 Key E slot pinout

Pin	Pin name	SOM pin	CPU pin	Description
1	GND			
2	VCC_3V3			
3	USB_DP			USB 2.0 D+ from the **USB_DN2** hub port
4	VCC_3V3			
5	USB_DN			USB 2.0 D- from the **USB_DN2** hub port
6	NC			
7	GND			
8	NC			
9	SDIO_CLK	T11	AF12	
10	NC			
11	SDIO_CMD	U10	AG12	
12	NC			
13	SDIO_DATA0	U11	AF14	
14	NC			
15	SDIO_DATA1	T9	AG13	
16	NC			
17	SDIO_DATA2	T10	AH13	
18	GND			
19	SDIO_DATA3	U9	AF13	
20	3V3_UART_WAKEn	M2	AA26	
21	SDIO_WAKEn	R1	AD30	
22	UART_TXD	U12	C22	M.2 TXD to SOM **M2E_RXD**
23	SDIO_RESETn	Y5	AE30	
24–31	Key E			Pins removed to act as physical key
32	UART_RXD	N3	F21	SOM **M2E_TXD** to M.2 RXD
33	GND			
34	UART_RTS	U6	C21	M.2 RTS to SOM **M2E_CTSn**
35	NC			
36	UART_CTS	D19	B21	SOM **M2E_RTSn** to M.2 CTS
37	NC			
38	VENDOR_DEFINED			**TCA9537** I/O expander P0
39	GND			
40	VENDOR_DEFINED			**TCA9537** I/O expander P1
41	NC			
42	VENDOR_DEFINED			**TCA9537** I/O expander P2
43	NC			
44	NC			
45	GND			
46	NC			
47	NC			
48	NC			
49	NC			
50	3V3_M2E_SUSCLK	M18	AF27	32.768 kHz SUSCLK in the 3.3 V domain
51	GND			
52	NC			
53	NC			
54	3V3_BT_DISABLEn	L2	AA25	
55	NC			
56	3V3_WF_DISABLEn	U17	AB28	
57	GND			
58	M2_SDA	A6	B2	1.8 V **MIPI_I2C** SDA through a 0 Ω link

Pin	Pin name	SOM pin	CPU pin	Description
59	NC			
60	M2_SCL	A8	A3	1.8 V MIPI_I2C SCL through a 0 Ω link
61	NC			
62	ALERTn			TCA9537 I/O expander P3
63	GND			
64	NC			
65	NC			
66	NC			
67	NC			
68	NC			
69	GND			
70	NC			
71	NC			
72	VCC_3V3			
73	NC			
74	VCC_3V3			
75	GND			
76	GND			

4.6 Camera Interface

The camera connector block routes a MIPI CSI-2 clock pair, two CSI data lanes, an I^2C control bus, and two camera GPIO signals. The connector is marked as **J7** and uses a horizontal ZIF FPC connector.

The control and GPIO signals are level-translated between **SOM_1V8_CTL** and the 3.3 V connector side through **LXS0104ZMAEX**.

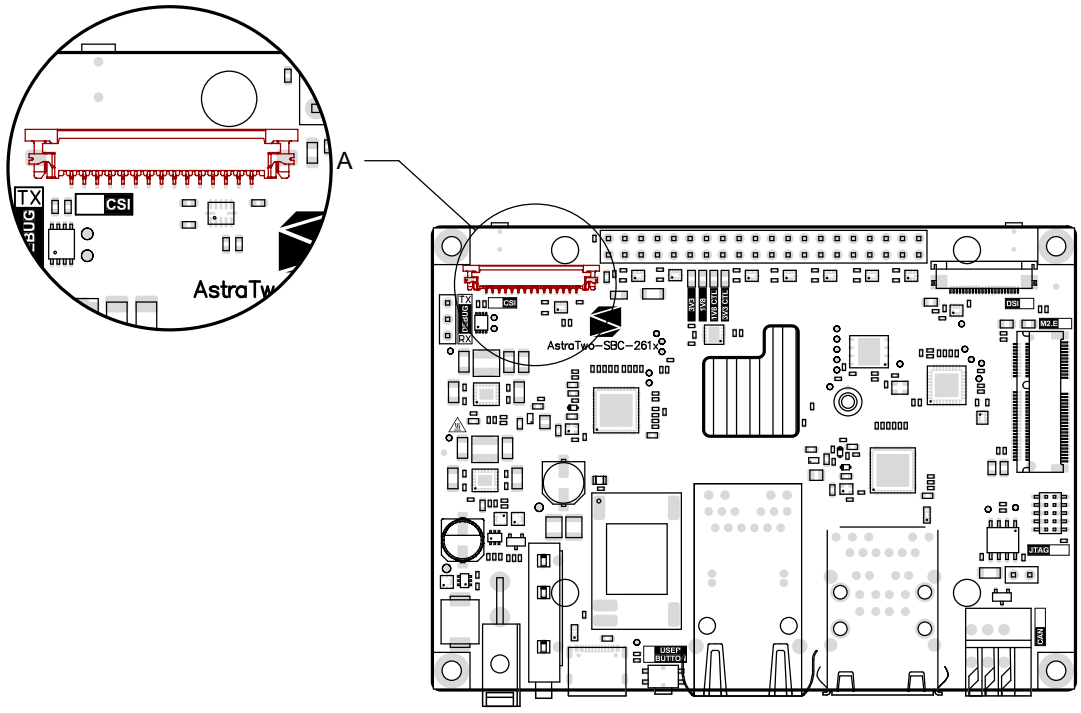


Fig. 8: Grinn AstraTwoSBC-261x MIPI CSI-2 camera connector location.

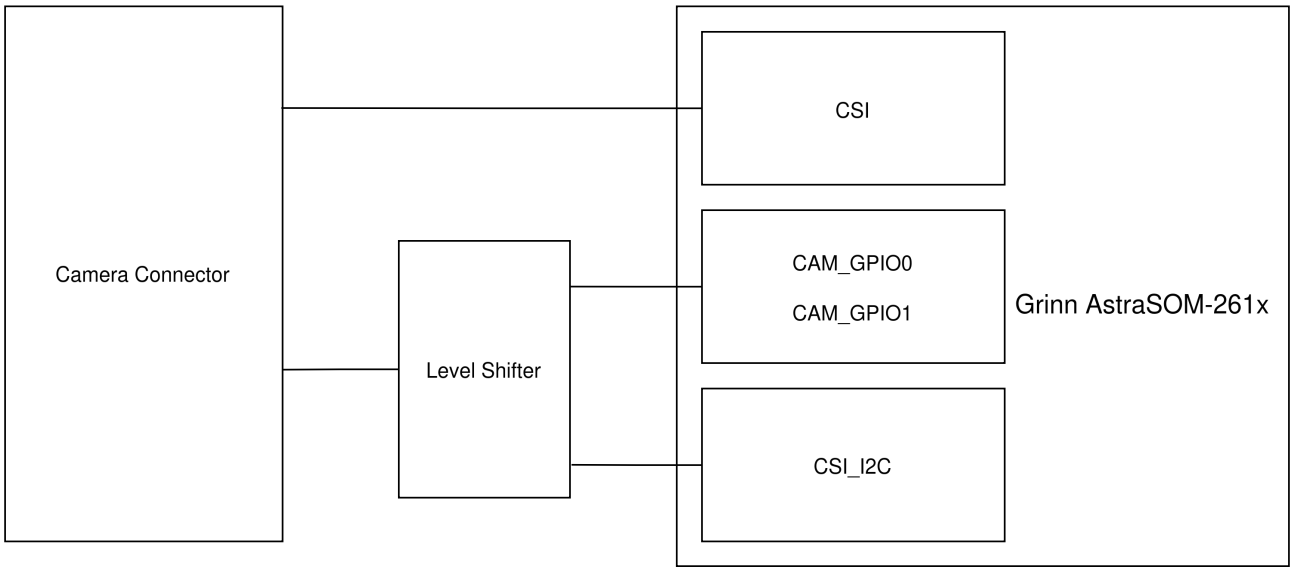


Fig. 9: Grinn AstraTwoSBC-261x camera interface block diagram.

Tab. 2: Grinn AstraTwoSBC-261x camera interface pinout

Pin	Pin name	SOM pin	CPU pin	Description
1	3V3			
2	CAM_SDA	A6	B2	
3	CAM_SCL	A8	A3	
4	IO1	P1	AC30	
5	IO0	N1	AC31	
6	GND			
7	CK_P	V11	AH19	
8	CK_N	Y11	AG19	
9	GND			
10	D1_P	V8	AG15	
11	D1_N	Y8	AG16	
12	GND			
13	D0_P	V9	AH17	
14	D0_N	Y9	AG17	
15	GND			

4.7 Display Interface

The display connector block routes a MIPI DSI clock pair, four DSI data lanes, an I²C control bus, and one SOM-controlled display GPIO signal. This GPIO path is named **DISPLAY_GPIO0** at board level and **DSI_GPIO0** on the display interface. The connector also exposes **DSI_GPIO1**, whose SOM-side translator input is routed to test point **TP18**. The connector is marked as **J8** and uses a top-contact ZIF FPC connector.

The display control signals are level-translated between **SOM_1V8_CTL** and the 3.3 V connector side through **LXS0104ZMAEX**.

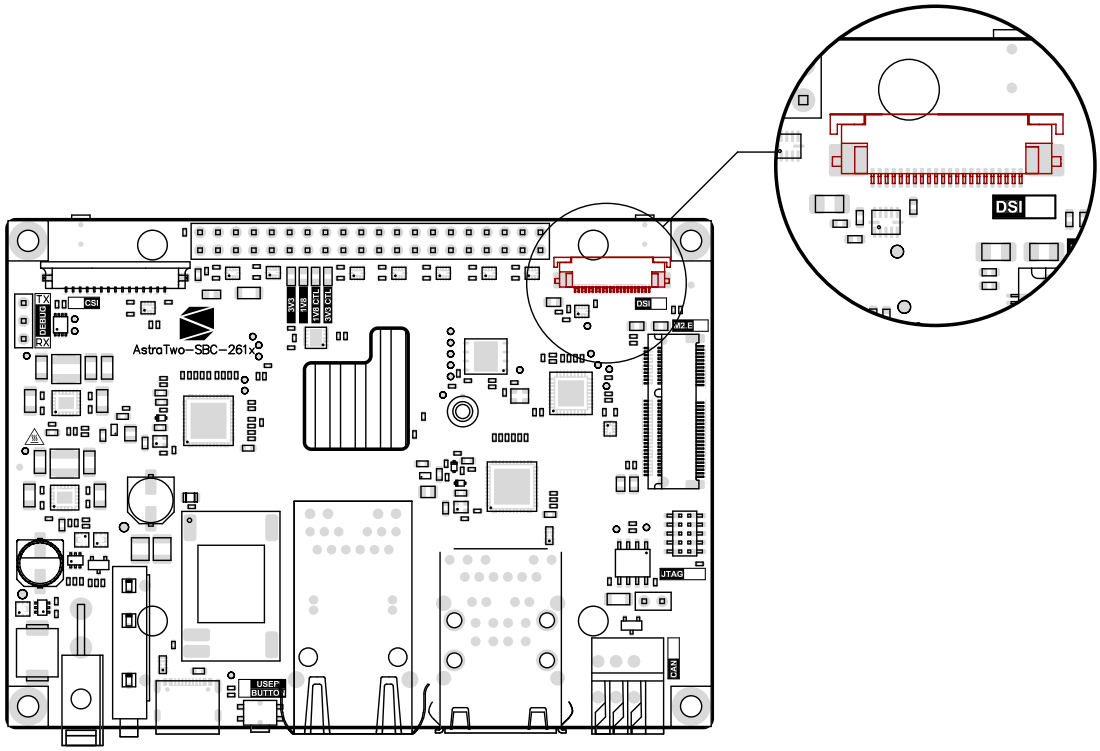


Fig. 10: Grinn AstraTwoSBC-261x MIPI DSI display connector location.

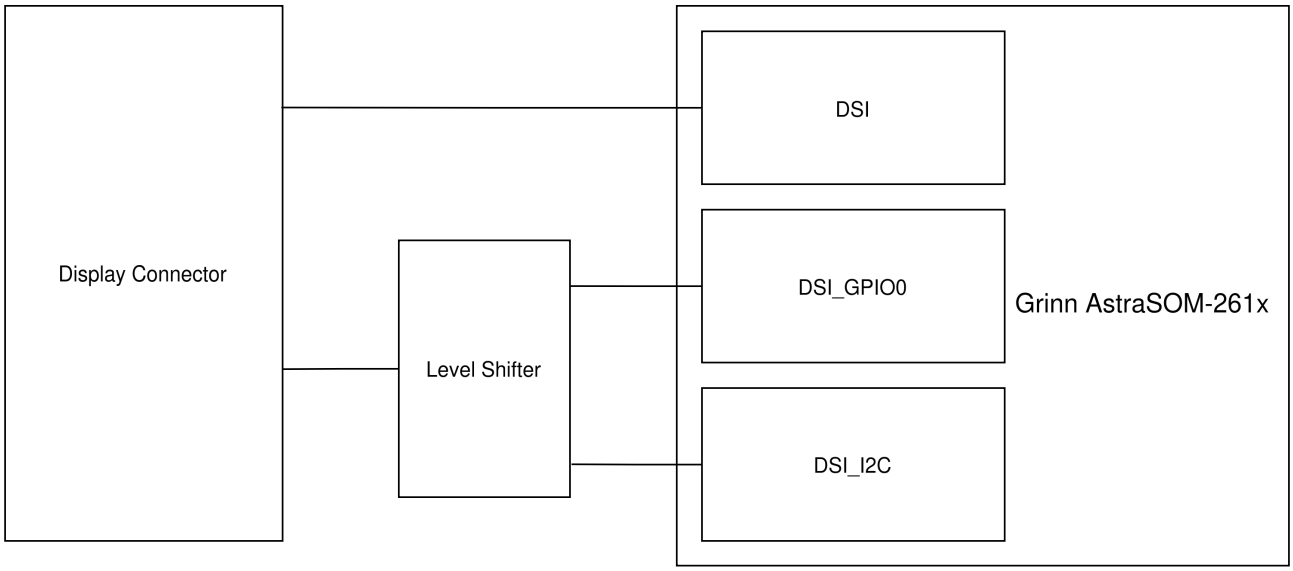


Fig. 11: Grinn AstraTwoSBC-261x display interface block diagram.

Tab. 3: Grinn AstraTwoSBC-261x display interface pinout

Pin	Pin name	SOM pin	CPU pin	Description
1	GND			
2	D0_N	Y18	AH26	
3	D0_P	V18	AG26	
4	GND			
5	D1_N	Y17	AG24	
6	D1_P	V17	AH24	
7	GND			
8	CK_N	Y15	AF24	
9	CK_P	V15	AF23	
10	GND			
11	D2_N	Y14	AH22	
12	D2_P	V14	AG22	
13	GND			
14	D3_N	Y12	AG21	
15	D3_P	V12	AG20	
16	GND			
17	DSI_GPIO0	F19	B25	Through 0 Ω link R83
18	DSI_GPIO1			SOM-side translator input is routed to TP18
19	GND			
20	DSI_SCL	A8	A3	
21	DSI_SDA	A6	B2	
22	3V3			

4.8 40-Pin Expansion Header

The 40-pin expansion header is marked as **J9**. GPIO signals are translated between the **SOM_1V8** domain and the 3.3 V header domain through **LXS0104ZMAEX** level translators. The header also exposes 5 V, 3.3 V, and GND pins. The default pinmux is configured in the Linux device tree to match the Raspberry Pi-style header functions.

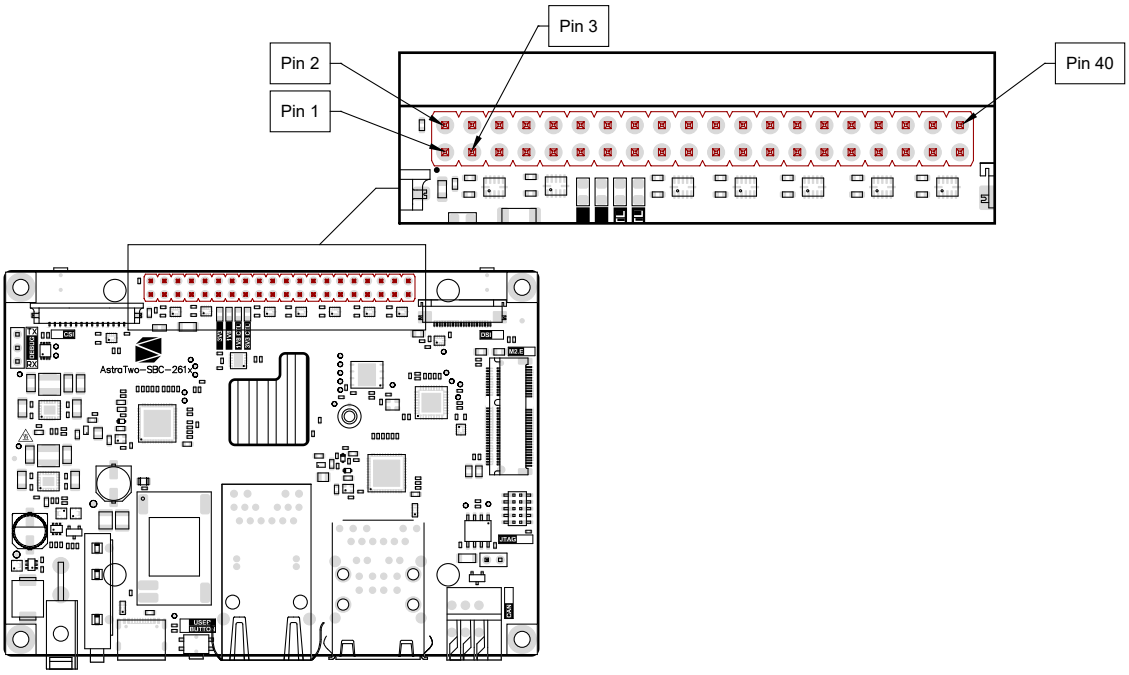


Fig. 12: Grinn AstraTwoSBC-261x 40-pin expansion header location.

Tab. 4: Grinn AstraTwoSBC-261x 40-pin expansion header pinout

Pin	Pin name	Default function	SOM pin	CPU pin	Description
1	3V3				
2	5V				
3	3V3_RPI_GPIO_2	I2C0_SDA	U5	U25	
4	5V				
5	3V3_RPI_GPIO_3	I2C0_SCL	V5	U28	
6	GND				
7	3V3_RPI_GPIO_4	GPIO	T1	C14	
8	3V3_RPI_GPIO_14	UART4_TXD	A8	A3	
9	GND				
10	3V3_RPI_GPIO_15	UART4_RXD	A6	B2	
11	3V3_RPI_GPIO_17	GPIO	A3	B6	
12	3V3_RPI_GPIO_18	I2S3_BCLK	T13	AC27	
13	3V3_RPI_GPIO_27	GPIO	A10	A6	
14	GND				
15	3V3_RPI_GPIO_22	GPIO	N18	K29	
16	3V3_RPI_GPIO_23	GPIO	L3	F19	
17	3V3				
18	3V3_RPI_GPIO_24	GPIO	T7	A21	
19	3V3_RPI_GPIO_10	SPI3_MOSI	H17	AA30	
20	GND				

Pin	Pin name	Default function	SOM pin	CPU pin	Description
21	3V3_RPI_GPIO_9	SPI3_MISO	H18	AB30	
22	3V3_RPI_GPIO_25	GPIO	M17	J29	
23	3V3_RPI_GPIO_11	SPI3_SCLK	G17	AA29	
24	3V3_RPI_GPIO_8	SPI3_CE0n	G18	AA31	
25	GND				
26	3V3_RPI_GPIO_7	SPI3_CE1n	G19	W29	
27	3V3_RPI_GPIO_0	I2C1_SDA	T4	A24	R8 links the SOM side to OPTIGA_SDA
28	3V3_RPI_GPIO_1	I2C1_SCL	U4	C24	R9 links the SOM side to OPTIGA_SCL
29	3V3_RPI_GPIO_5	GPIO	L17	H30	
30	GND				
31	3V3_RPI_GPIO_6	GPIO	N19	M29	
32	3V3_RPI_GPIO_12	GPIO	C19	D22	
33	3V3_RPI_GPIO_13	GPIO	J19	B22	
34	GND				
35	3V3_RPI_GPIO_19	I2S3_FS	T14	AE24	
36	3V3_RPI_GPIO_16	GPIO	P18	P26	
37	3V3_RPI_GPIO_26	GPIO	R18	L29	R109 links the SOM side to M2_INT_EXP
38	3V3_RPI_GPIO_20	I2S3_DIN	U14	AC25	
39	GND				
40	3V3_RPI_GPIO_21	I2S3_DOUT	U13	AF30	

4.9 CAN

The CAN interface is connected to **CAN0_TX** and **CAN0_RX** from the SOM and uses a **TCAN1044V** transceiver. The interface includes:

- **CAN_H** and **CAN_L** bus signals
- 120 Ω termination resistor **R38**, disconnected by removing jumper **J11**
- Terminal block **J10** with **CAN_H**, **CAN_L**, GND, and 24 V pins

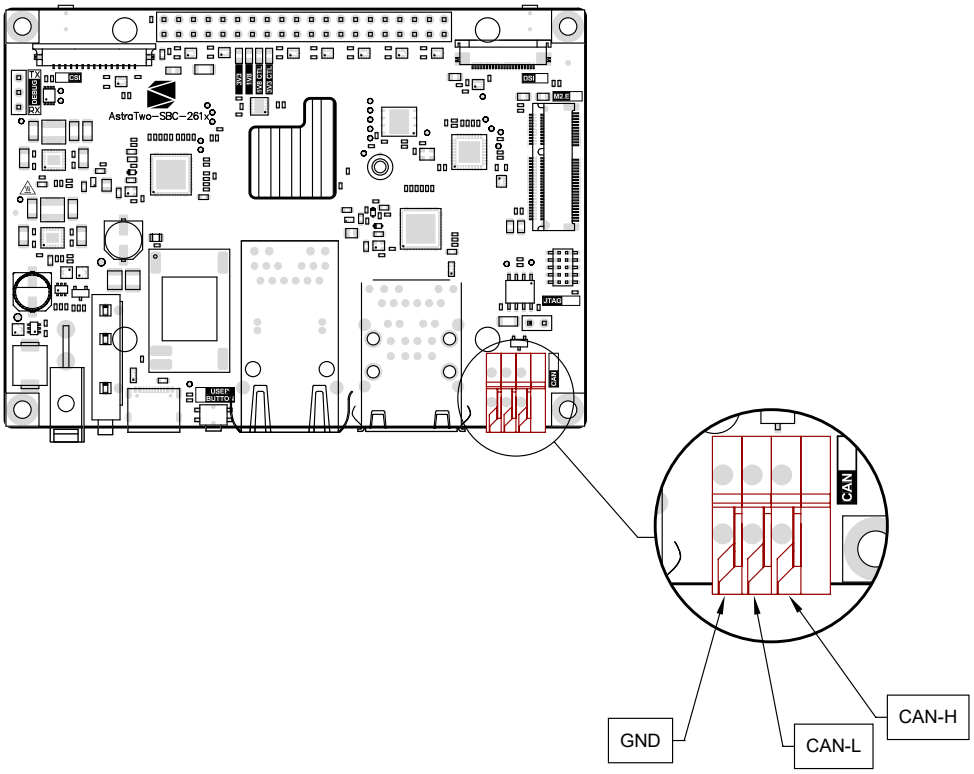


Fig. 13: Grinn AstraTwoSBC-261x CAN connector location.

4.10 OPTIGA™ Trust M Security Module

The Grinn AstraTwoSBC-261x is equipped with the Infineon OPTIGA™ Trust M SLS32AIA010M, a hardware security module designed to support advanced security use cases in embedded systems and IoT applications.

This discrete secure element enables a wide range of security functions, including:

- Secure storage of cryptographic keys and certificates
- Hardware-accelerated RSA and ECC cryptographic operations
- Mutual authentication and secure TLS channel establishment
- Device identity protection and attestation
- Platform integrity verification
- Tamper-resistant key provisioning

The module connects to the main processor over an I²C interface and operates independently of the host system, enabling isolated execution of cryptographic functions. It complies with Common Criteria EAL6+ (hardware) and supports X.509 certificates for identity and authentication tasks.

I²C Interface Configuration

- **I²C Bus:** OPTIGA_I2C (SM_TW1)
- **I²C Address:** `0x30` (7-bit)

Tab. 5: OPTIGA™ Trust M I²C Pinout

Pin	Signal	CPU Pin	SOM Pin
SDA	OPTIGA_SDA	T4	A24
SCL	OPTIGA_SCL	U4	C24
RSTn	Optiga_RSTn	F1	A13

Its integration on the Grinn AstraTwoSBC-261x makes it a robust choice for applications requiring strong trust anchors, such as secure boot, encrypted firmware updates, cloud onboarding, and secure communications in industrial or consumer-grade devices.

> **Warning**
>
> The OPTIGA™ Trust M security module does *not* respond to standard I²C scan tools such as `i2cdetect`, because it does not acknowledge general read requests. To verify its presence on the bus or communicate with it, use the Infineon-provided tool `trustx_scan` instead.

4.11 JTAG

The Cortex JTAG connector is marked as **J12**. It exposes **VTref**, GND, **SM_TRSTn**, **SM_TMS**, **SM_TCK**, **SM_TDO**, **SM_TDI**, and **RESETn**.

> **Note**
>
> When selecting an adapter for a J-Link Base probe, verify that it routes **RESETn** to pin 10 of **J12**. An adapter without this connection cannot provide debugger-controlled board reset.

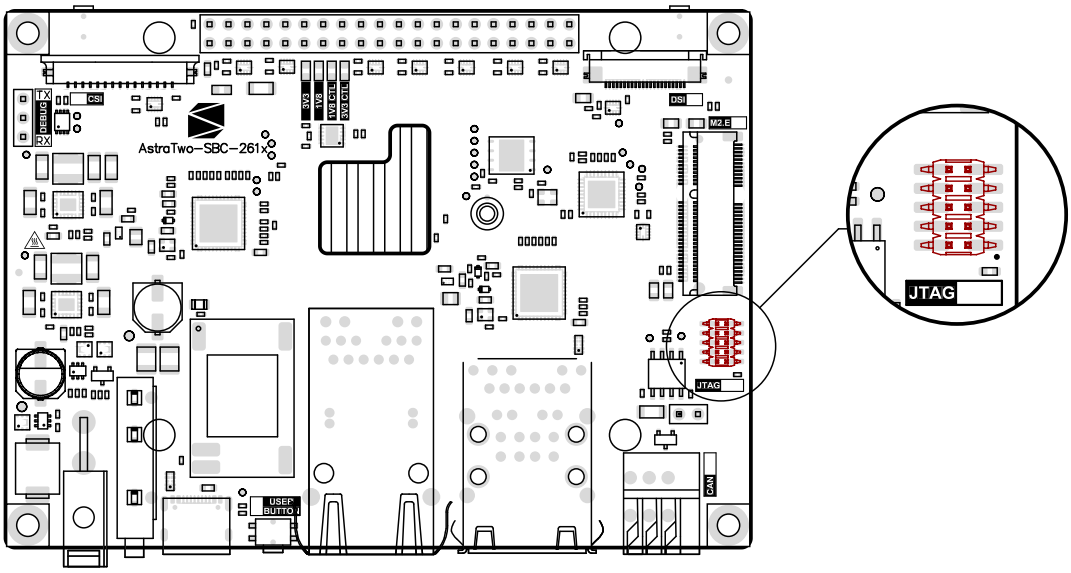


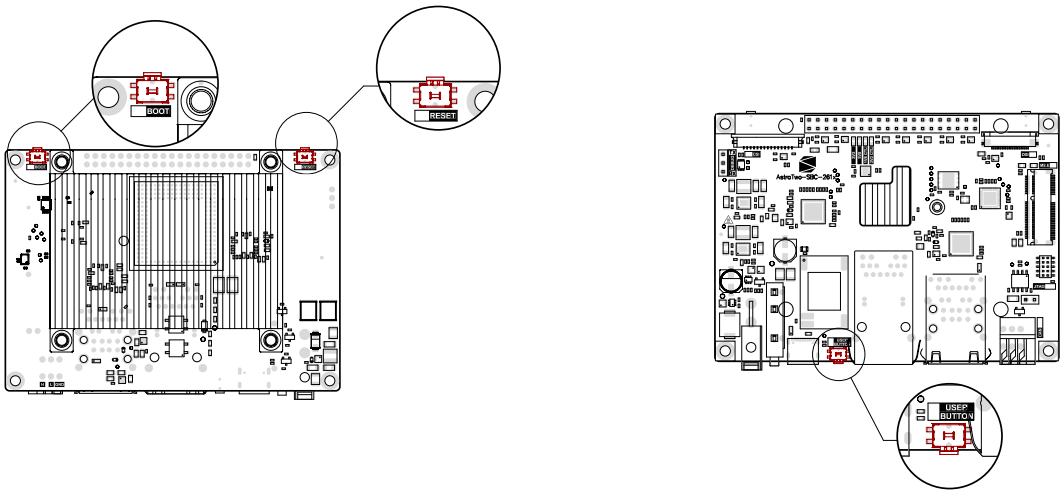
Fig. 14: Grinn AstraTwoSBC-261x JTAG connector location.

Tab. 6: Grinn AstraTwoSBC-261x JTAG connector pinout

Pin	Cortex signal	Board signal	SOM pin	CPU pin
1	VTref	SOM_1V8 via R88		
2	TMS	SM_TMS	F17	V30
3	GND	GND		
4	TCK	SM_TCK	J18	W30
5	GND	GND		
6	TDO	SM_TDO	J17	U30
7	NC	NC		
8	TDI	SM_TDI	E17	T30
9	DETn	SM_TRST	P3	W26
10	RESETn	RESETn	Y6	U29

4.12 User Interface

The Grinn AstraTwoSBC-261x provides a set of user interface components for controlling and monitoring the board during development and integration.



(a) BOOT and RESET button locations. **(b)** USER button location.

Fig. 15: Grinn AstraTwoSBC-261x button locations.

4.12.1 Boot Button (BOOT)

The **BOOT** button (S2) is used to control the boot mode of the Grinn AstraTwoSBC-261x during power-up or reset.

This button is typically used in conjunction with the **RESET** button during software updates or recovery procedures.

4.12.2 Reset Button (RESET)

The **RESET** button (S1) performs a hard reset of the SOM. Pressing it will restart the SOM without removing power, and it resets all peripherals and processor state. It is commonly used to recover from software hangs or to restart the board after flashing new firmware.

4.12.3 User Button (USER)

The **USER** button (S3) is software-defined. It is connected to SOM pin `E18` (CPU pin `SM_GPIO10`). Its behavior is not fixed in hardware and can be assigned by firmware or user-space software (e.g., triggering application actions, diagnostics, or a safe-shutdown handler via a GPIO interrupt).

4.12.4 LED Indicators

The board includes three user defined LEDs:

- **D18 (red LED)** – Power status LED connected to SOM pin `A7` (CPU pin `GPIO24`); default software trigger: `default-on`.
- **D19 (green LED)** – Disk activity LED connected to SOM pin `A9` (CPU pin `GPIO23`); default software trigger: `mmc0`.
- **D20 (yellow LED)** – Heartbeat LED connected to SOM pin `K17` (CPU pin `GPIO22`); default software trigger: `heartbeat`.

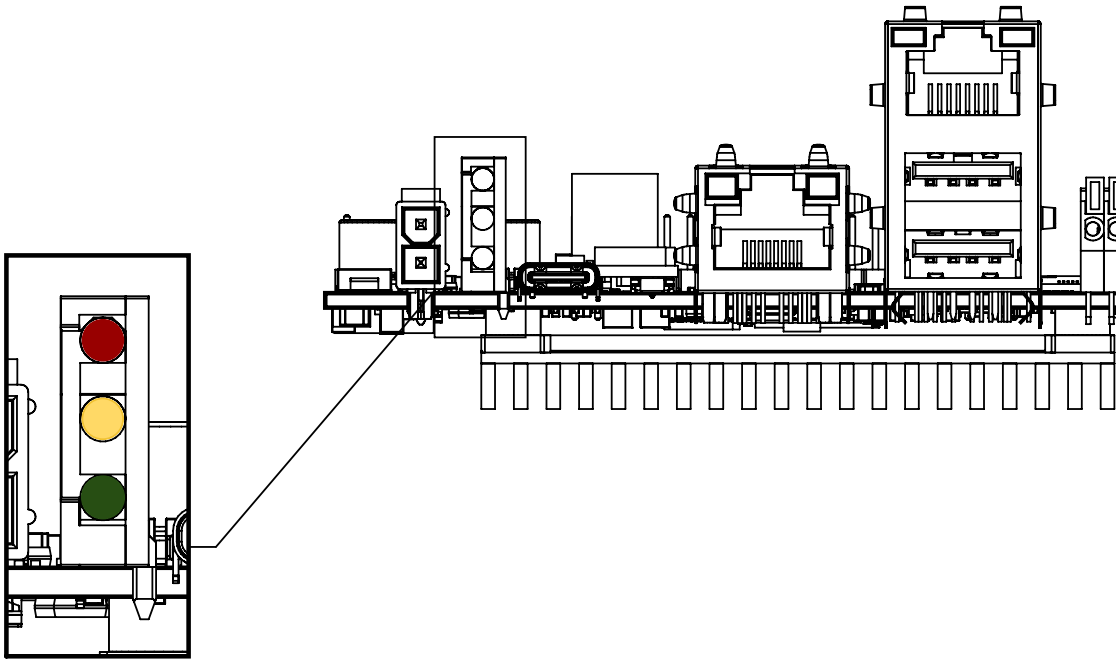


Fig. 16: Grinn AstraTwoSBC-261x LED indicator locations.

5 Boot Options

The default boot source for Grinn AstraTwoSBC-261x is eMMC. The boot source is selected by the SOM-domain **BOOT_SRC[1:0]** strap state.

Tab. 7: Boot source strap states.

Boot device	BOOT_SRC[1]	BOOT_SRC[0]
USB 2.0	Low	Low
xSPI NOR	Low	High
eMMC	High	Low
xSPI NAND	High	High

5.1 Default Boot

The default assembly is configured for eMMC boot. During normal operation, the board loads the bootloader and operating system image from eMMC.

5.2 Boot from On-board SPI NOR

Grinn AstraTwoSBC-261x can also boot from the on-board SPI NOR flash. The SPI NOR device is **U27** (**GD25LQ128E**, 128 Mbit) and is connected to the SOM xSPI interface.

To boot from SPI NOR, select the **xSPI NOR** state shown in Tab. 7 and program a valid boot image into the NOR flash.

5.3 Supported OS

Grinn AstraTwoSBC-261x supports Grinn Linux images based on the Yocto Project. Platform integration resources are available from the meta-grinn-astra repository.

5.4 Flashing Mode

The board exposes **BOOTn**, **RESETn**, the USB-C 2.0 device port, and the CLI UART. A typical flashing sequence is:

1. Apply board power through the main input or supported PoE input path.
2. Connect the USB-C 2.0 device/debug port to the host PC.
3. Hold the BOOT button or assert **BOOTn**.
4. Press and release RESET.
5. Release BOOT after the host-side flashing tool detects the device.

> **Note**
>
> Detailed flashing instructions are available in the Developer Portal.

5.5 Serial Console

A dedicated **CLI_UART** interface is routed through the debug header circuitry. The UART signals use 3.3 V logic levels. Use a 3.3 V logic-level USB-to-UART adapter.

Tab. 8: Initial serial console settings.

Parameter	Value
Baud rate	115200
Data bits	8
Parity	None
Stop bits	1
Flow control	None

6 Electrical Characteristics

6.1 Recommended Operating Conditions

Tab. 9: Grinn AstraTwoSBC-261x recommended operating conditions

Parameter	Minimum	Typical	Maximum	Unit
Supply voltage VIN	10.8	12–24	26	V
Supply current	0.5	2	3	A
Operating ambient temperature	-40	25	+85	°C

7 Mechanical Characteristics

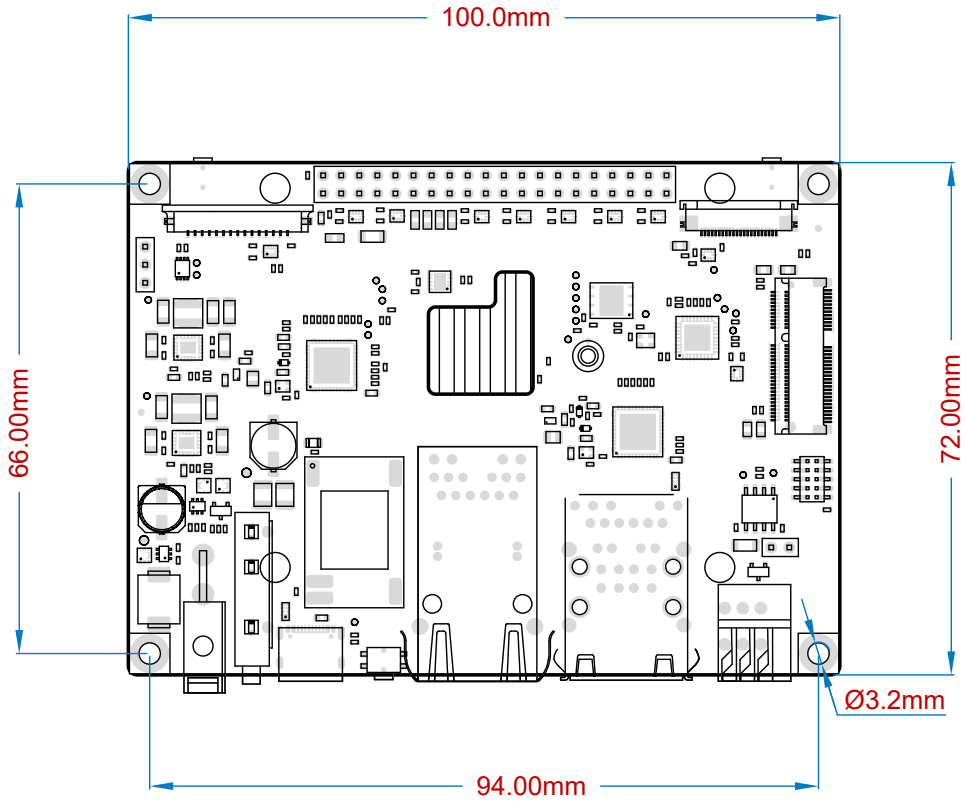
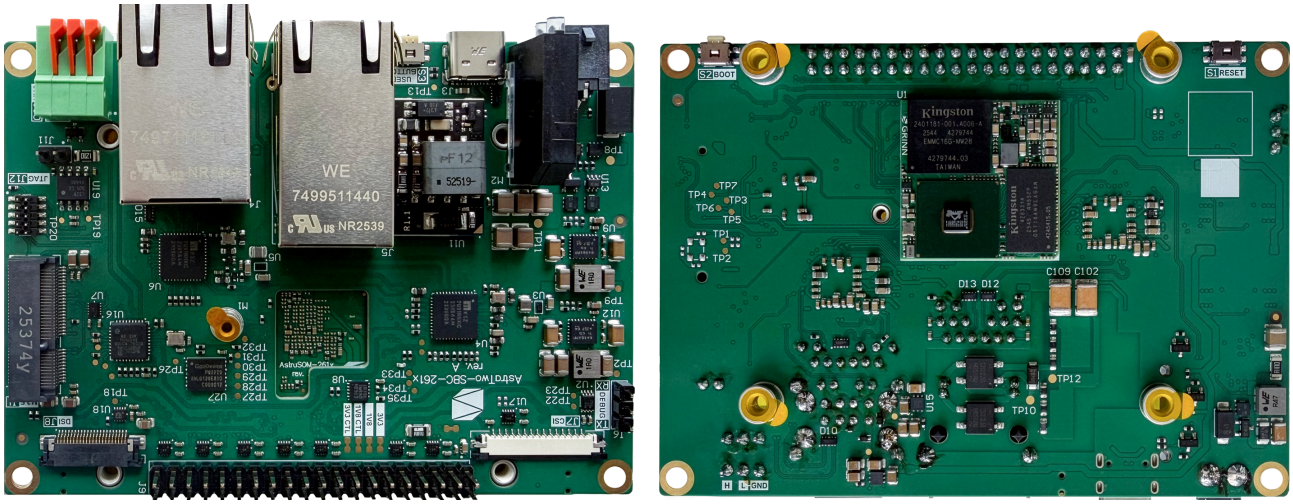


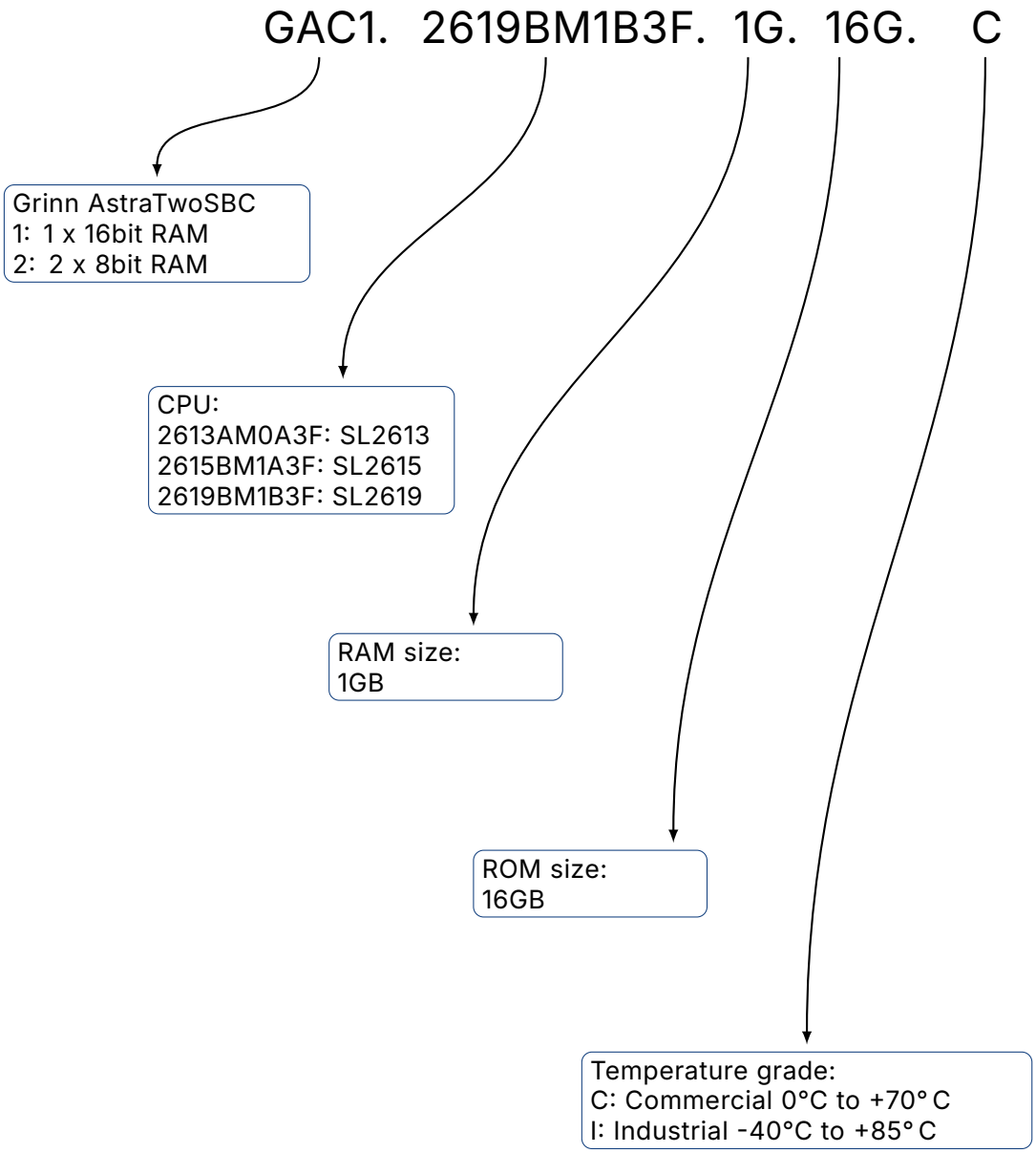
Fig. 17: Grinn AstraTwoSBC-261x board dimensions



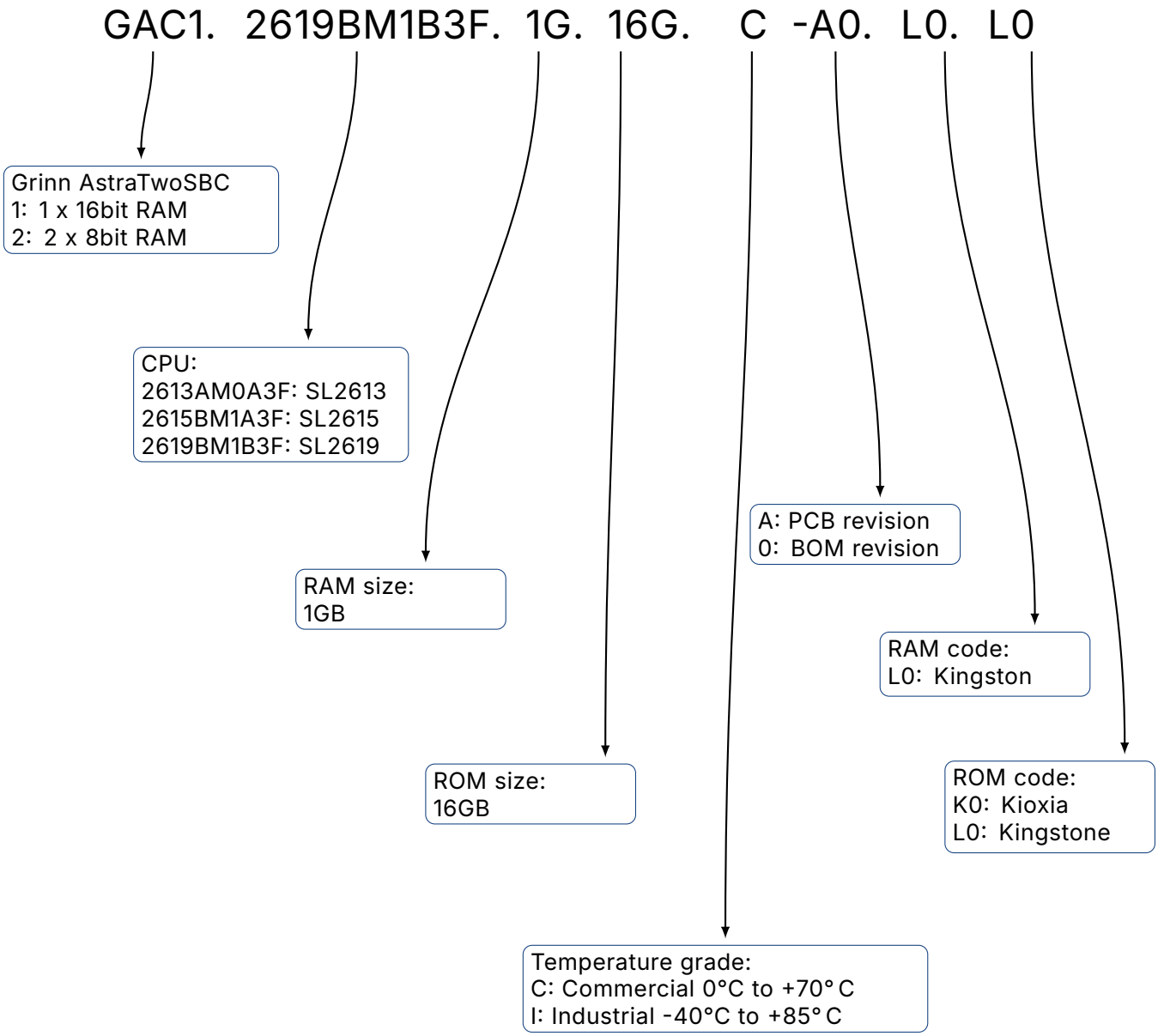
(a) top view **(b)** bottom view (without radiator)

Fig. 18: Grinn AstraTwoSBC-261x board views

8 Ordering Part Number



9 Full Part Number



9.1 Detailed Information on RAM Codes

Tab. 10: Detailed RAM code information.

Code	Manufacturer	Part Number
L0	Kingston	D5116AN9CXGXN-UF

9.2 Detailed Information on ROM Codes

Tab. 11: Detailed ROM code information.

Code	Manufacturer	Part Number
K0	Kioxia	THGAMVG7T13BAIL
L0	Kingston	EMMC16G-MW28-03010

Revision History

Revision	Date	Description
1.0	2026-08-03	Initial release.

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