GRINN

Datasheet

Grinn GenioBoard - Edge AI SBC

Getting Started Guide | Prebuilt Images | Developer Resources | Customer Support

1 Features

- Ideal for prototyping and early development
- OPTIGA™ Trust M SLS32AIA010M security module for hardware-based key storage and cryptographic operations
- Single-cable USB development interface — includes programming and CLI access
- Single power supply input with a USB-C Power Delivery (PD) interface
- Supports both Grinn GenioSOM-510 and Grinn GenioSOM-700 system-on-modules
- Raspberry Pi HAT-compatible interface
- HDMI and DisplayPort (DP) interfaces
- 10/100/1000 Mbps Ethernet PHY with RGMII interface
- M.2 M PCIe x1 Gen2 for AI accelerators
- M.2 E for WiFi & Bluetooth modules
- 4 pin fan connector
- 2x USB-A 2.0
- 2x USB-A 3.0
- Built-in USB-C to UART interfaces
- 2x CSI 4 lane camera interfaces
- 4GB RAM (up to 8GB) & 16GB eMMC

2 Applications

- AI-supported computer vision applications
- Advanced IoT devices
- Smart home applications
- Industrial automation
- Streaming audio and video
- Multimedia applications

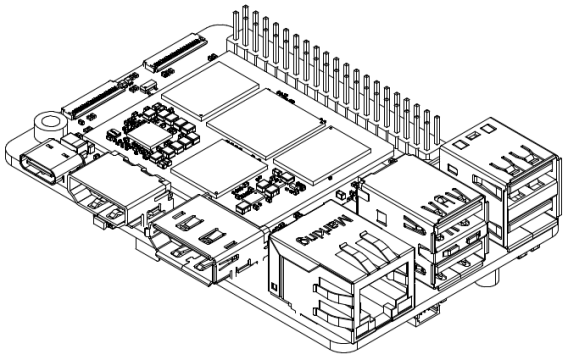
3 Description

Grinn GenioBoard is a compact and versatile single board computer (SBC) built around the Grinn GenioSOM module. It is designed to accelerate development by providing direct access to all key interfaces and peripherals available on the module, enabling rapid prototyping for embedded applications.

Grinn GenioBoard is intended for professional use in laboratory, development, evaluation, and integration environments by highly qualified technicians or engineers. The system integrator is responsible for the design, validation, regulatory compliance, safety assessment, and cybersecurity hardening of any final product developed using the Grinn GenioBoard or derived reference designs.

To support security-critical applications, Grinn GenioBoard includes Infineon's OPTIGA™ Trust M SLS32AIA010M security module, which provides secure key storage and hardware-accelerated cryptographic operations for authentication, secure communication, and platform integrity protection.

With industrial-grade I/O, a robust feature set, and comprehensive reference documentation, Grinn GenioBoard serves as an ideal starting point for custom carrier board development and system integration using the Grinn GenioSOM.



Contents

4 Functional Description

4.1 Power Supply

The Grinn GenioBoard features a modern power distribution system designed for efficiency, flexibility, and reliability. It is powered via a USB-C connector supporting USB Power Delivery (USB PD), managed by the integrated Texas Instruments TPS25730D PD controller. The system supports a wide input voltage range from 5V to 20V, allowing operation under diverse power sources.

For full functionality of all onboard peripherals and interfaces, a 60W USB PD power supply is recommended. However, typical applications require only around 6W. The power subsystem includes high-efficiency buck converters as well as linear regulators, ensuring stable voltage rails with low noise and optimal thermal performance. The system supports up to 5A current under maximum load conditions.

Note

Powering the board with 5V via a USB-A to USB-C cable (i.e., without USB PD negotiation) may result in insufficient power delivery. This can lead to instability or limited functionality of certain high-power peripherals.

Warning

In the event of a short circuit on the 3.3V or 5.0V power rails, the onboard DC/DC converters will enter a protection state and will not restart automatically. Restoring normal operation requires a complete power cycle of the system, including disconnecting and reapplying the USB-C power source.

Warning

If the ambient temperature exceeds 30 °C, the combined power drawn from the 3.3V and 5V rails must not exceed 20 W (total). Exceeding this limit may result in thermal overstress of the onboard DC/DC converters and can lead to reduced reliability or board shutdown.

Warning

During operation, especially under high computational and I/O load or elevated ambient temperature, certain PCB areas and components may reach high surface temperatures.
Allow the board to cool down before handling. Avoid direct contact with heat-generating components.

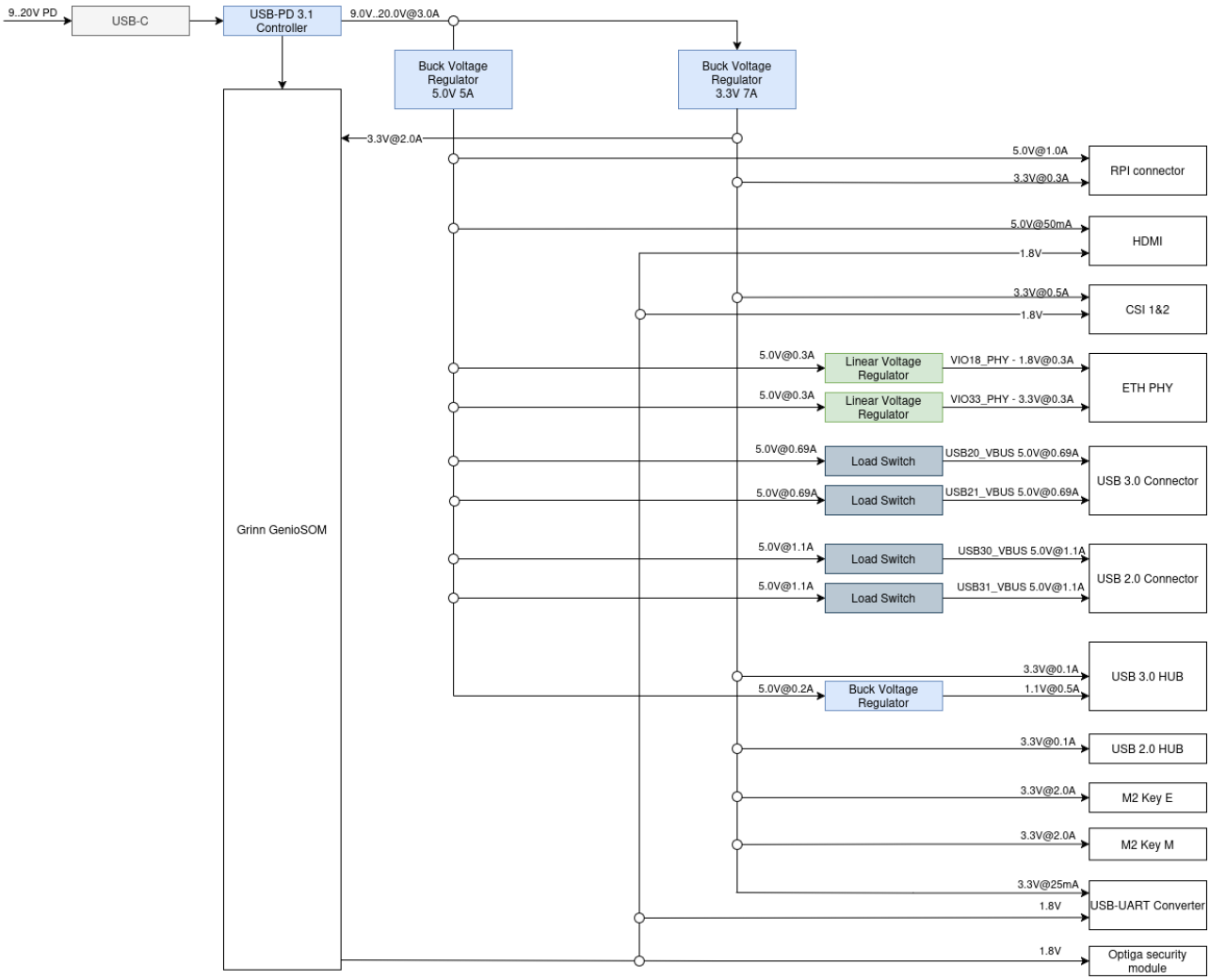


Fig. 1: Grinn GenioBoard PSU diagram

4.2 External Cabling Recommendations

External cable selection has a direct impact on the overall EMC performance of the system. To improve robustness during immunity testing and in typical integration scenarios, the use of appropriately selected cable types and lengths is recommended for all external interfaces connected to the Grinn GenioBoard.

For USB-C, HDMI, and DisplayPort connections, cable lengths should not exceed 3 m. For Ethernet connectivity, the cable length should not exceed 30 m, and shielded Ethernet cabling shall be used.

4.2.1 40 PIN Header

The Grinn GenioBoard supports the 40 PIN connector, as shown in the schematic below. All pins are 3.3V compatible. The interface is based on the TXS0108 devices, which require correct signal routing to operate reliably. These translators can exhibit improper behavior when connected through long wire harnesses or when the signal integrity is otherwise degraded. In unfavorable cases, an output may enter an oscillation state, which typically appears as an averaged voltage of approximately 1.65 V when measured with a multimeter. Pull-downs on the translated GPIO lines are not recommended, as they can interfere with the device's internal one-shot circuitry.

For detailed electrical guidance and design constraints, refer to the official Texas Instruments documentation for the TXS0108.

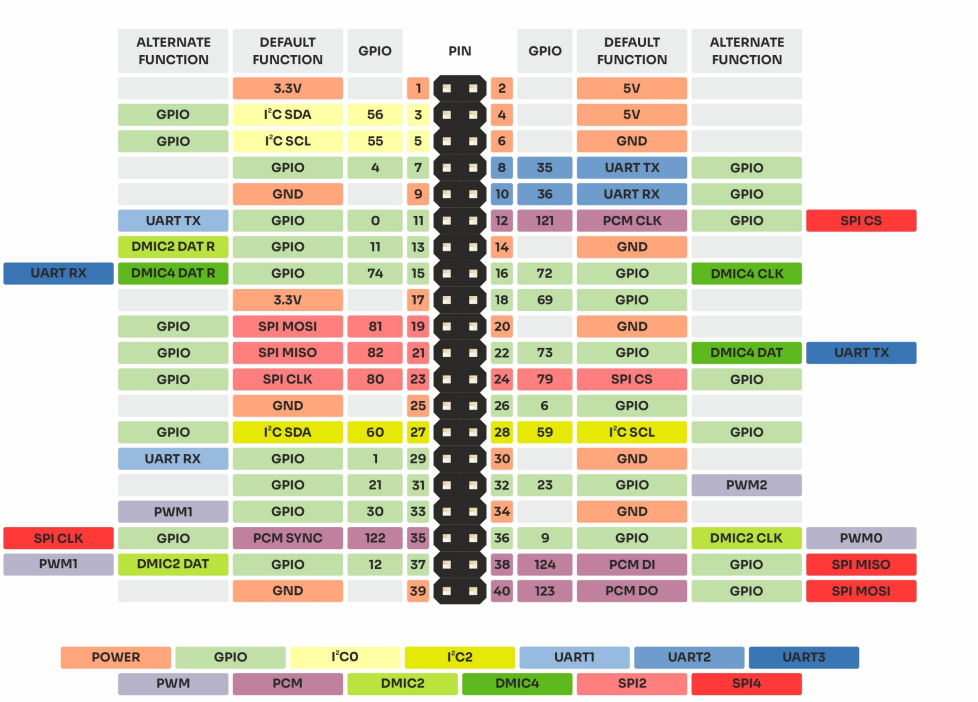


Fig. 2: 40 PIN Header schematic

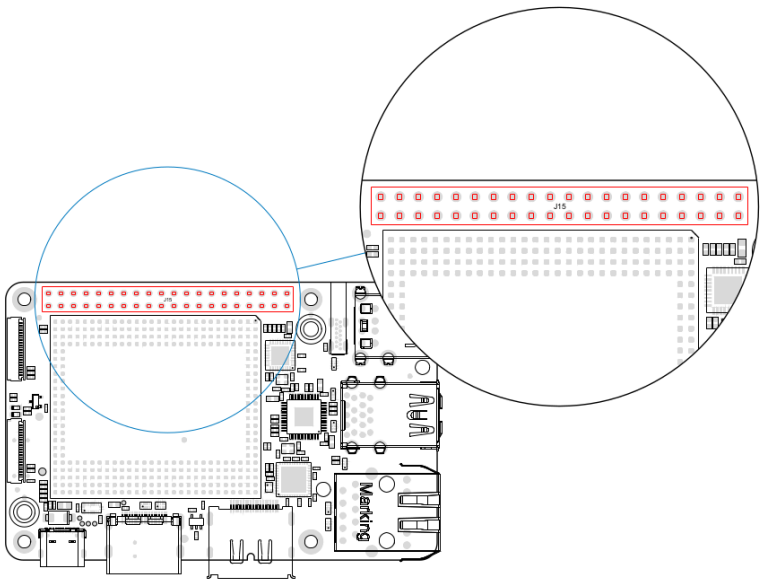


Fig. 3: Grinn GenioBoard 40 PIN Header

Tab. 1: Grinn GenioBoard 40 PIN Header functions

Pin	Default function	Alternate function 1	Alternate function 2
1	3.3V		
2	5V		
3	I2C SDA	GPIO 56	
4	5V		
5	I2C SCL	GPIO 55	
6	GND		
7	GPIO 4		
8	UART TX	GPIO 35	
9	GND		
10	UART RX	GPIO 36	
11	GPIO 0	UART RX	
12	PCM CLK	GPIO 121	SPI CS
13	GPIO 11	DMIC2 DAT R	
14	GND		
15	GPIO 74	DMIC4 DAT R	UART RX
16	GPIO 72	DMIC4 CLK	
17	3.3V		
18	GPIO 69		
19	SPI MOSI	GPIO 81	
20	GND		
21	SPI MISO	GPIO 82	
22	GPIO 73	DMIC4 DAT	UART TX
23	SPI CLK	GPIO 80	
24	SPI CS	GPIO 79	
25	GND		
26	GPIO 6		
27	I2C SDA	GPIO 60	
28	I2C SCL	GPIO 59	
29	GPIO 1	UART RX	
30	GND		
31	GPIO 21		
32	GPIO 30	PWM2	
33	GPIO 33	PWM1	
34	GND		
35	PCM SYNC	GPIO 122	SPI CLK
36	GPIO 9	DMIC2 CLK	PWM0
37	GPIO 12	DMIC2 DAT	PWM1
38	PCM DI	GPIO 124	SPI MISO
39	GND		
40	PCM DO	GPIO 123	SPI MOSI

4.3 Video Interfaces

4.3.1 HDMI

The Grinn GenioBoard is equipped with a full-size HDMI output driven by the MediaTek MT8390 / MT8370 processor on Grinn GenioSOM. The HDMI transmitter complies with the HDMI 2.0b standard and offers extensive support for high-resolution video and multi-channel audio formats.

- Resolutions up to 4096×2160p @ 60 Hz (8-bit mode)
- Deep Color support up to 16-bit
- Color formats: RGB 4:4:4, YCbCr 4:4:4, 4:2:2, 4:2:0, xvYCC
- 3D video support
- HDCP 1.4 and 2.3 content protection
- HDR with dynamic metadata (up to 2 KB)
- CEC (Consumer Electronics Control)
- Embedded audio support:
  - LPCM up to 8 channels
  - S/PDIF IEC61937 and IEC60958 (up to 192 kHz, 24-bit)
  - DSD (Direct Stream Digital)
  - Support for compressed lossless formats

4.3.2 DisplayPort

The DisplayPort interface on the Grinn GenioBoard is compliant with the DisplayPort 1.4 specification and enables high-performance video output.

- Up to 4 lanes at 5.4 Gbps per lane (HBR3)
- Resolutions up to 3840×2160 (4K2K) @ 60 Hz, 10-bit
- Color formats: RGB 8/10-bit, YUV422, YUV444 (8/10-bit)
- HDCP 1.3 and 2.2 content protection
- Display Stream Compression (DSC)
- HDR and Adaptive Sync support
- DP AUX channel for link management and configuration

These display interfaces enable high-quality video output for external displays and multimedia terminals in both consumer and industrial environments.

> **Note**
>
> Pin 20 of the DisplayPort connector on the Grinn GenioBoard provides no power (DP_PWR), therefore active DP cables or adapters requiring power on this pin are not supported.

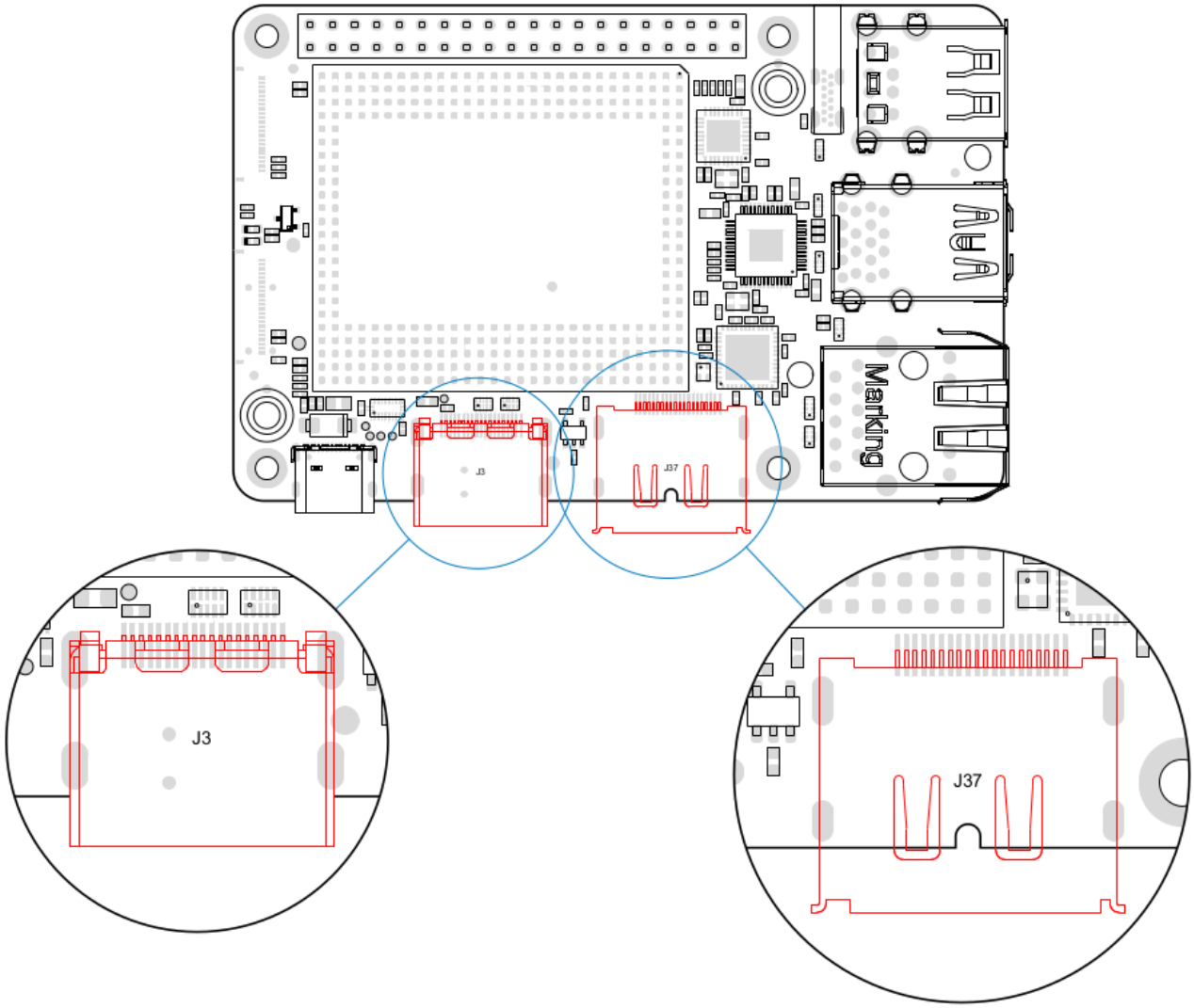


Fig. 4: Grinn GenioBoard video outputs

4.4 OPTIGA™ Trust M Security Module

The Grinn GenioBoard is equipped with the Infineon OPTIGA™ Trust M SLS32AIA010M, a hardware security module designed to support advanced security use cases in embedded systems and IoT applications.

This discrete secure element enables a wide range of security functions, including:

- Secure storage of cryptographic keys and certificates
- Hardware-accelerated RSA and ECC cryptographic operations
- Mutual authentication and secure TLS channel establishment
- Device identity protection and attestation
- Platform integrity verification
- Tamper-resistant key provisioning

The module connects to the main processor over an I²C interface and operates independently of the host system, enabling isolated execution of cryptographic functions. It complies with Common Criteria EAL6+ (hardware) and supports X.509 certificates for identity and authentication tasks.

I²C Interface Configuration

- **I²C Bus:** I2C6
- **I²C Address:** `0x30` (7-bit)

Tab. 2: OPTIGA™ Trust M I²C Pinout

Pin	Signal	CPU Pin	SOM Pin
SDA	I2C6.SDA	I2C6_SDA	A7
SCL	I2C6.SCL	I2C6_SCL	B7
RSTn	OPTIGA_RESETn	MSDC1_DATA2	A10

Its integration on the Grinn GenioBoard makes it a robust choice for applications requiring strong trust anchors, such as secure boot, encrypted firmware updates, cloud onboarding, and secure communications in industrial or consumer-grade devices.

> **Warning**
>
> The OPTIGA™ Trust M security module does *not* respond to standard I²C scan tools such as `i2cdetect`, because it does not acknowledge general read requests. To verify its presence on the bus or communicate with it, use the Infineon-provided tool `trustx_scan` instead.

4.4.1 CSI

The Grinn GenioBoard board includes two 4-lane CSI interfaces, each capable of supporting a maximum bit rate of **2.5 Gbps per lane**. Camera sub-boards connect to the board using the WR-FPC 687122182122 connector.

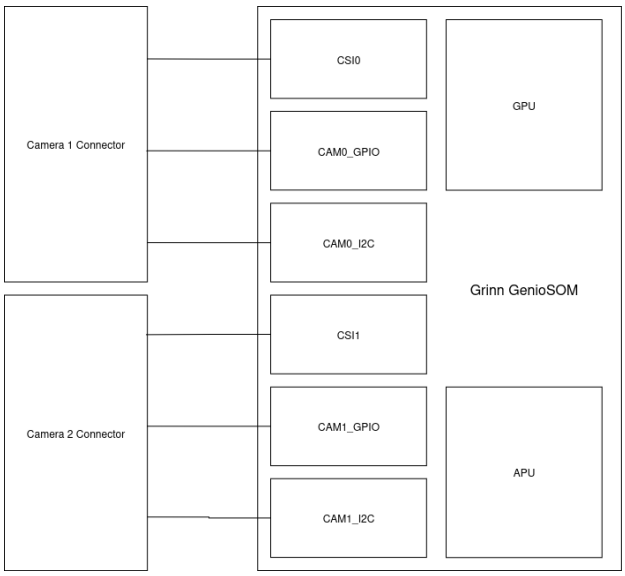


Fig. 5: Grinn GenioBoard CSI diagram

Tab. 3: Grinn GenioBoard CSI camera connectors

Pin	Camera 1 Signal	Camera 2 Signal
1	GND	GND
2	CSI0A_L0_N	CSI1A_L0_N
3	CSI0A_L0_P	CSI1A_L0_P
4	GND	GND
5	CSI0A_L1_N	CSI1A_L1_N
6	CSI0A_L1_P	CSI1A_L1_P
7	GND	GND
8	CSI0A_L2_N	CSI1A_L2_N
9	CSI0A_L2_P	CSI1A_L2_P
10	GND	GND
11	CSI0B_L0_N	CSI1B_L0_N
12	CSI0B_L0_P	CSI1B_L0_P
13	GND	GND
14	CSI0B_L1_N	CSI1B_L1_N
15	CSI0B_L1_P	CSI1B_L1_P
16	GND	GND
17	CAM0_GPIO0	CAM1_GPIO0
18	CAM0_GPIO1	CAM1_GPIO1
19	GND	GND
20	I2C5.SCL	I2C3.SCL
21	I2C5.SDA	I2C3.SDA
22	3V3	3V3

Warning

Make sure to insert the FPC cable in the correct orientation. Pay close attention to the **"Pin 1"** marking on GRINN FPC cable — improper insertion may damage the camera.

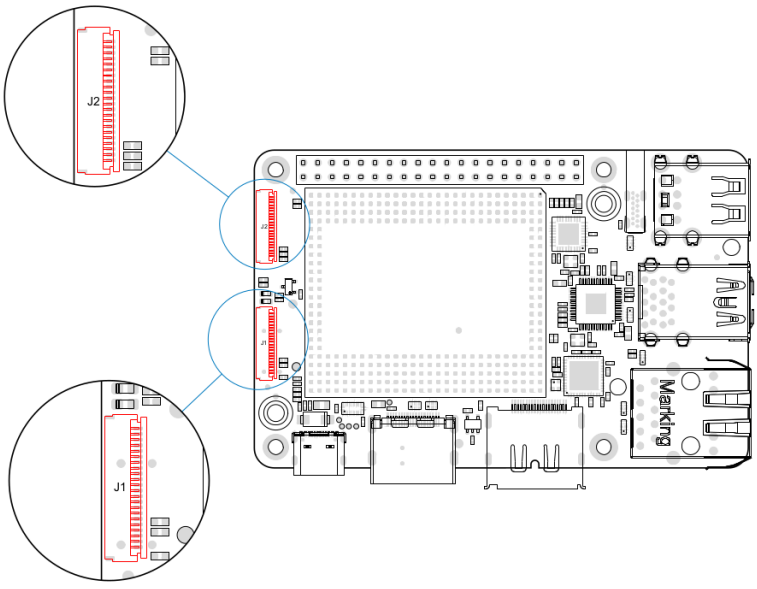


Fig. 6: Grinn GenioBoard CSI camera connectors

4.5 M.2 Connectors

The Grinn GenioBoard is equipped with two M.2 connectors for system expansion:

- **M.2 E-key slot** – intended for Wi-Fi and Bluetooth modules
- **M.2 M-key slot** – designed for AI accelerators over PCIe

The M.2 E-key slot supports USB connectivity for wireless modules; however, PCIe is not available on this connector. The remaining pins follow the standard M.2 E-key layout.

The M.2 M-key slot supports only a single PCIe lane (x1) and does not support SATA-based devices.

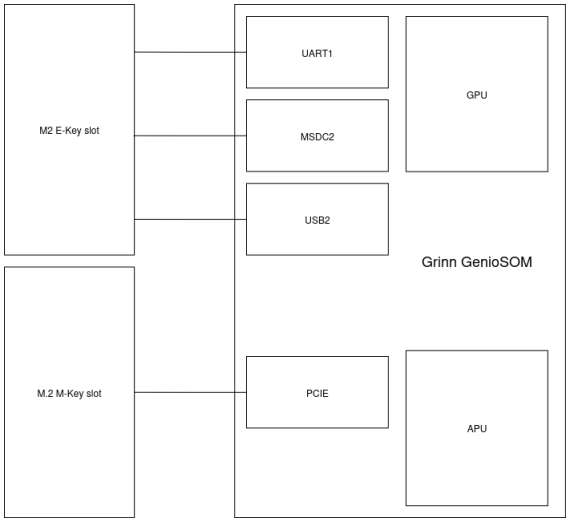


Fig. 7: Grinn GenioBoard M.2 diagram

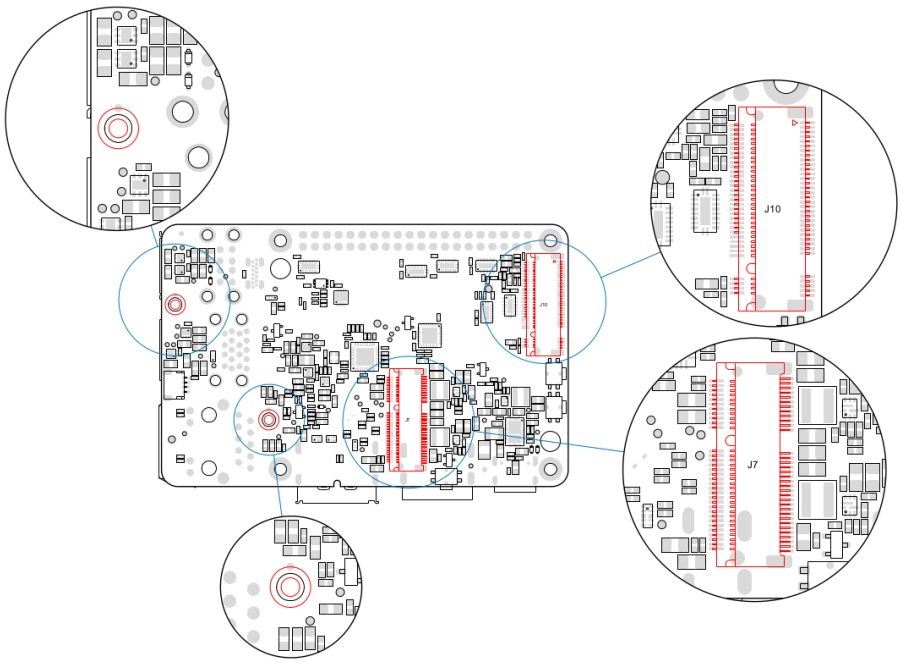


Fig. 8: Grinn GenioBoard M.2 connectors

Tab. 4: Grinn GenioBoard Wi-Fi/BLE M.2 Key E slot pinout

Pin	Pin name	Description
1	GND	
2	3.3V	
3	USB.D_P	
4	3.3V	
5	USB.D_N	
6	NC	
7	GND	
8	NC	
9	MSDC2.CLK	
10	NC	
11	MSDC2.CMD	
12	NC	
13	MSDC2.DATA0	
14	NC	
15	MSDC2.DATA1	
16	NC	
17	MSDC2.DATA2	
18	GND	
19	MSDC2.DATA3	
20	UART_WAKEn_3V3	
21	SDIO_WAKEn	
22	UART1.RXD	
23	SDIO_RESETn	
24-31	Key E	Pins removed to act as physical key
32	UART1.TXD	
33	GND	
34	UART1.CTSn	
35	NC	
36	UART1.RTSn	
37	NC	
38	NC	
39	GND	
40	NC	
41	NC	
42	NC	
43	NC	
44	NC	
45	GND	
46	NC	
47	NC	
48	NC	
49	NC	
50	SUSCLK_32k	Oscillator 32.768kHz
51	GND	
52	NC	
53	NC	
54	BT_DISABLEn_3V3	
55	NC	
56	WIFI_DISABLEn_3V3	
57	GND	

Continued on next page

Table 4 – continued from previous page

Pin	Pin name	Description
58	NC	
59	NC	
60	NC	
61	NC	
62	NC	
63	GND	
64	NC	
65	NC	
66	NC	
67	NC	
68	NC	
69	GND	
70	NC	
71	NC	
72	3.3V	
73	NC	
74	3.3V	
75	GND	
76	GND	

Tab. 5: Grinn GenioBoard PCIe M.2 Key M slot pinout

Pin	Pin name	Description
1	GND	
2	3.3V	
3	GND	
4	3.3V	
5	NC	
6	NC	
7	NC	
8	NC	
9	GND	
10	NC	
11	NC	
12	3.3V	
13	NC	
14	3.3V	
15	GND	
16	3.3V	
17	NC	
18	3.3V	
19	NC	
20	NC	
21	GND	
22	NC	
23	NC	
24		
25	NC	
26		
27	GND	

Continued on next page

Table 5 – continued from previous page

Pin	Pin name	Description
28		
29	NC	
30		
31	NC	
32	NC	
33	GND	
34	NC	
35	NC	
36	NC	
37	NC	
38	NC	
39	GND	
40	NC	
41	PCIE.RX_N	
42	NC	
43	PCIE.RX_P	
44	NC	
45	GND	
46	PCM_DI	
47	PCIE_C_TX0_N	
48	PCM_CLK	
49	PCIE_C_TX0_P	
50	PCIE_PERSTn_3V3	
51	GND	
52	PCIE_CLKREQn_3V3	
53	PCIE.CK_N	
54	PCIE_WAKEn_3V3	
55	PCIE.CK_P	
56	NC	
57	GND	
58	NC	
59–66	Key M	Pins removed to act as physical key
67	NC	
68	NC	
69	NC	
70	3.3V	
71	GND	
72	3.3V	
73	GND	
74	3.3V	
75	GND	
76	GND	

4.5.1 DEEPX DX-M1 M.2 Module

The DEEPX DX-M1 M.2 Module is an extenal AI accelerator that enhances the Grinn GenioBoard AI performance when higher inference throughput is required.

The module integrates the DEEPX DX-M1 SoC, delivering 25 TOPS of native INT8 compute (equivalent to 200 eTOPS). It features a dedicated deep-learning accelerator architecture with an integrated high-bandwidth memory subsystem and supports model conversion from TensorFlow, ONNX, Keras, and PyTorch through the DEEPX dataflow compiler.

Thermal operating limits are –25°C to +85°C with throttling, and –25°C to +65°C without throttling. Power consumption ranges from 2 W (minimum) to 5 W (maximum) when running DEEPX-optimized AI models.

The module interfaces with the Grinn GenioBoard via the PCIe Gen2 x2 link provided on the M.2 Key M slot (J3). Mechanical mounting is supported by the integrated M3 standoffs.

The DX-M1 supports a wide range of state-of-the-art neural networks, including ResNet, MobileNet v1–v3, EfficientNet, EfficientDet, SSD, YOLOv5/7/8 and later variants, DeepLabv3, PIDNet, and vision-language models such as CLIP, enabling high-performance inference for embedded vision, robotics, and edge-AI systems.

> **Note**
>
> The Grinn GenioBoard can be ordered with the DEEPX DX-M1 module pre-installed. See Section 8 for detailed ordering information.

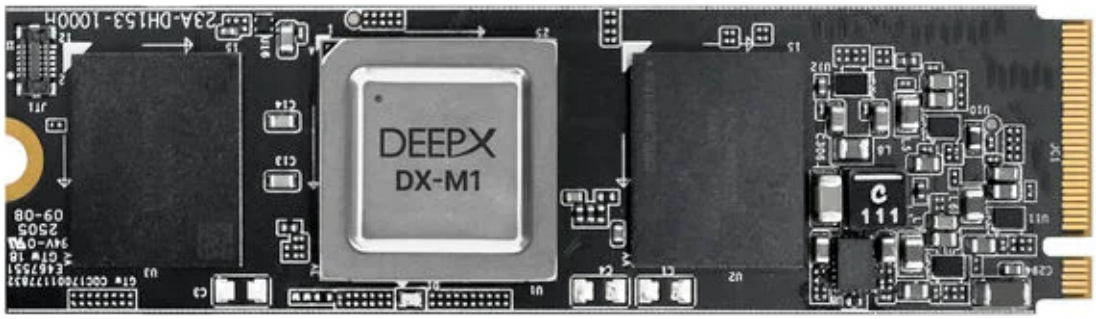


Fig. 9: DX-M1 M.2 Module

4.6 Ethernet

The Grinn GenioBoard includes an onboard 10/100/1G Ethernet transceiver, the Microchip KSZ9031RNXI. The Ethernet PHY interfaces with the Grinn GenioSOM via an RGMII interface.

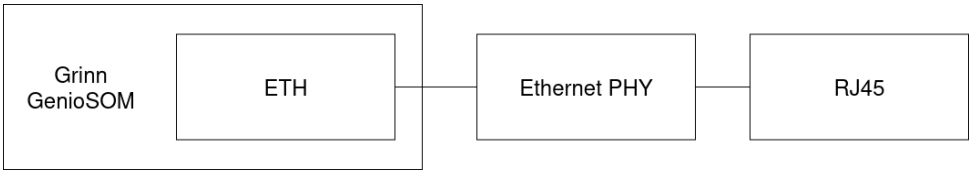


Fig. 10: Grinn GenioBoard Ethernet diagram

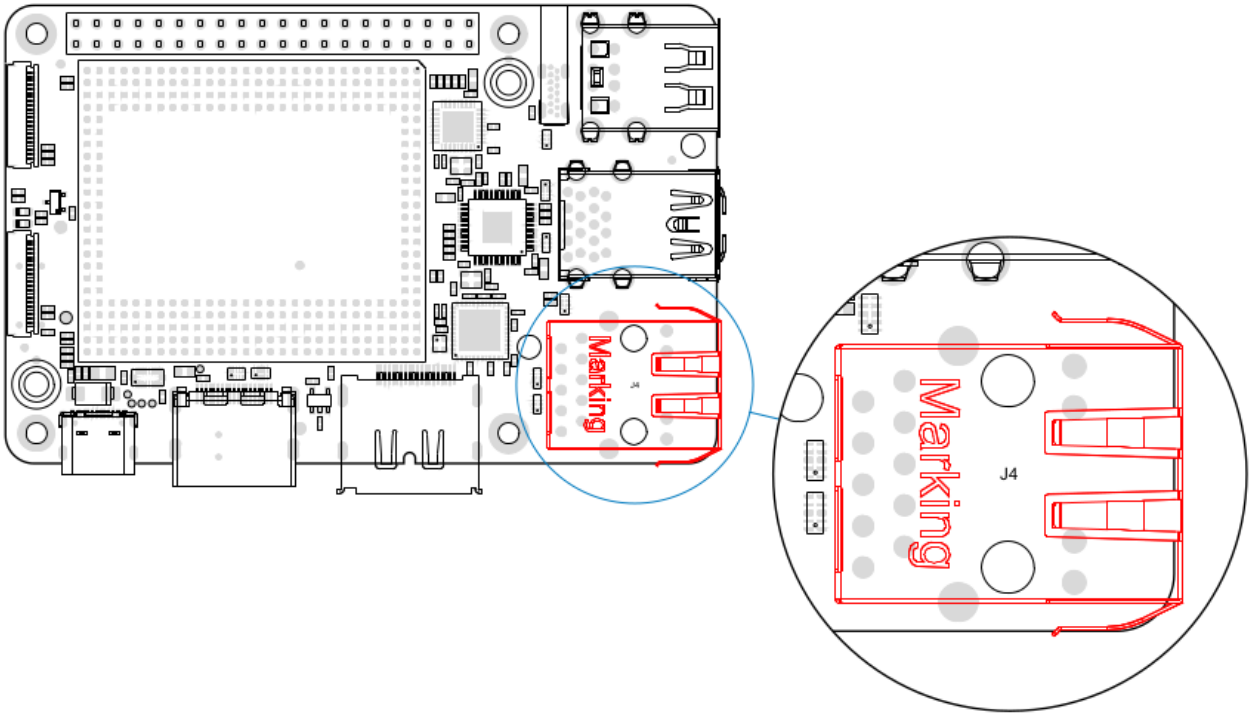


Fig. 11: Grinn GenioBoard Ethernet connector placement

4.7 USB Architecture

The Grinn GenioBoard provides a flexible USB subsystem based on three USB interfaces routed from the Grinn GenioSOM: USB0, USB1, and USB2. These are distributed through multiple hubs to support a wide range of peripherals.

4.7.1 USB0 – Debug and Console Interface

USB0 is dedicated to debug and console functionality. It is connected to the downstream (DN) port of a USB 2.0 hub, while the upstream (UP) port of the hub is connected to the PC host via USB-C port. There is also USB to UART converter connected to downstream port. For more information refer Section 5.3.

4.7.2 USB1 – High-Speed I/O

USB1 is connected to a USB 3.0 hub and provides:

- Two USB-A 3.0 ports for high-speed devices such as storage or cameras

This interface supports USB 3.0 bandwidth and is suitable for demanding peripherals.

4.7.3 USB2 – Peripheral and Wireless Expansion

USB2 is routed to a 3-port USB 2.0 hub, which provides:

- Two USB-A 2.0 ports for standard peripherals
- One connection routed internally to the M.2 E-key slot for Wi-Fi/Bluetooth modules

This design enables simultaneous use of external USB devices and internal wireless modules, maintaining compatibility and bandwidth balance.

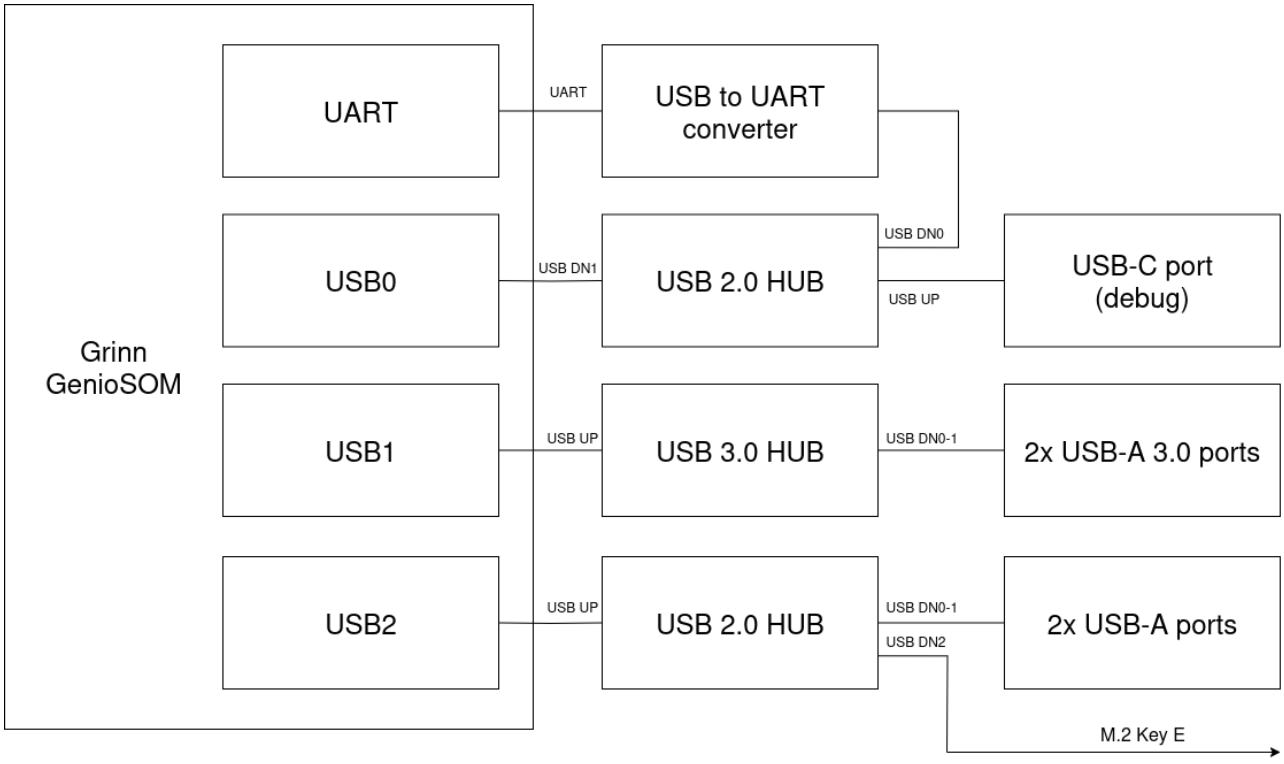


Fig. 12: Grinn GenioBoard USB architecture

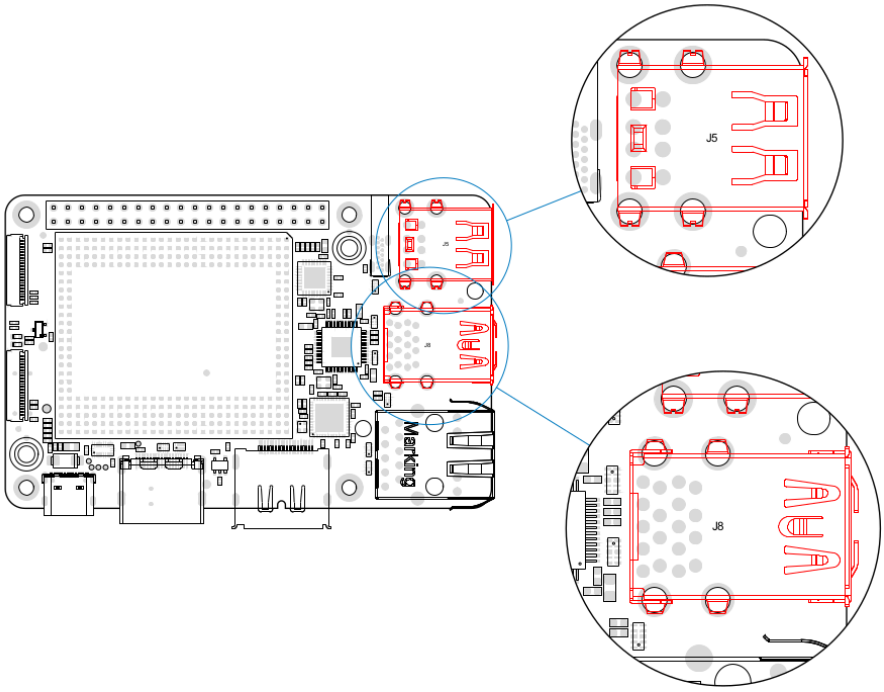


Fig. 13: Grinn GenioBoard USB connector placement

4.8 User Interface

The Grinn GenioBoard provides a set of user interface components for controlling and monitoring the board during development and integration.

4.8.1 Reset Button (RESET)

The **RESET** button performs a hard reset of the SOM. Pressing it will restart the SOM without removing power, and it resets all peripherals and processor state. It is commonly used to recover from software hangs or to restart the board after flashing new firmware.

4.8.2 Download Button (DOWNLOAD)

The **DOWNLOAD** button is used to enter firmware flashing mode. It is typically used in combination with the RESET button to put the SOM into download mode for the flashing tool to recognize the device. For detailed instructions, refer to Section 5, subsection 5.2.

4.8.3 LED Indicators

The board includes two status LEDs:

- **D14 (green LED)** – Indicates the presence of 3.3V power. Connected to the 3.3V power domain and lights up when the board is powered.
- **D15 (red LED)** – General-purpose LED connected to SOM pin `AJ7` (CPU pin `DPI_CK`). It can be toggled via software and used as a status, activity, or debug indicator.

5 Boot options

The Grinn GenioBoard can be booted from eMMC. Flashing is performed via the USB-C (J11) port using the Mediatek genio-flash tool.

5.1 Supported OS

The Grinn GenioBoard supports a custom Linux Yocto build and Debian. To obtain access to the Git repository, please contact `support@grinn-global.com`.

5.2 Flashing

To flash the Grinn GenioBoard, one needs a Linux, Windows or MAC host PC with AIoT Tools installed, a power adapter, and a USB-C cable.

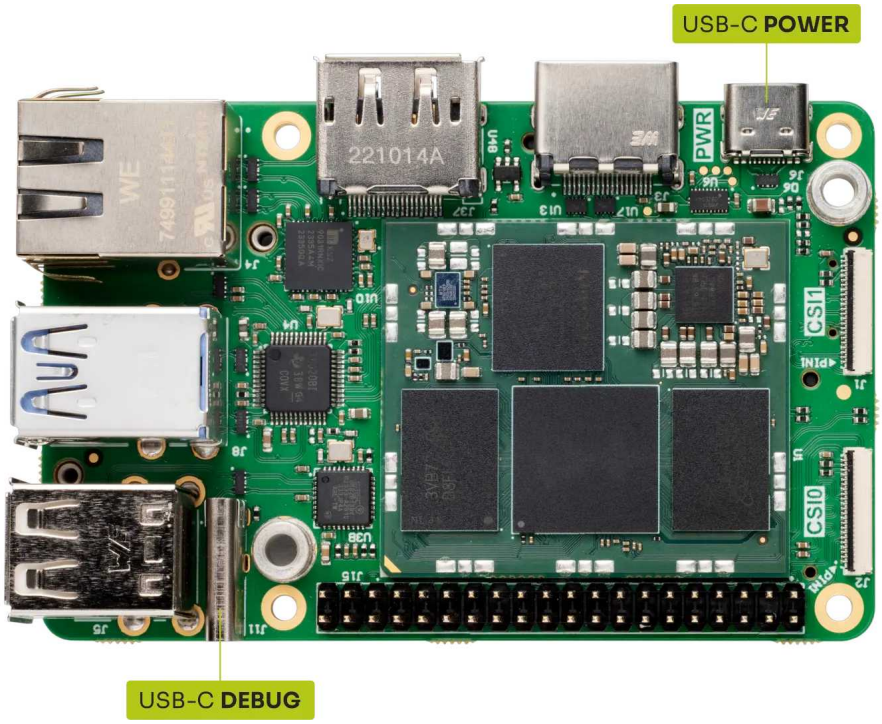


Fig. 14: Grinn GenioBoard USB debug & power placement

Here's a high-level overview of the process:

- Connect the Board: Use the power adapter to power the board and connect the board to the host PC via the USB-C port.
- Launch the Flash Tool: Navigate to the directory containing the image files and run the `genio-flash` command with the necessary device tree blob overlays.
- Enter Download Mode: Follow these steps:
  - Press and hold the DOWNLOAD (S3) button.
  - Press and release the RESET (S2) button.
  - Continue holding the DOWNLOAD button until the "Erasing 'mmc0" message appears in the log.

You can find a more detailed description of the process in the Getting Started Guide

5.3 CLI Access

The Grinn GenioBoard exposes two serial interfaces via the USB-C debug port (USB0), each appearing as a different device node on the host PC. These provide access to different firmware components during the boot process and at runtime.

5.3.1 `/dev/ttyACMx` – UART0 (Boot Rom)

This interface is connected to the SoC's UART0 and provides early debug output from the Little Kernel (LK), as well as other low-level debug messages. It is particularly useful during early boot stages and firmware development. The configuration is:

- Baud rate: `115200`
- Data bits: `8`
- Parity: `None`
- Stop bits: `1`

5.3.2 `/dev/ttyUSBx` – Linux or U-Boot Shell or Preboot

This interface provides access to the main serial console of the board. Depending on the boot stage, it gives access to either the U-Boot command line or the Linux login shell or Preboot. It uses the following settings:

- Baud rate: `921600`
- Data bits: `8`
- Parity: `None`
- Stop bits: `1`

> **Note**
>
> Serial port names may vary depending on the operating system. For example, on Windows, they appear as `COMx` instead of `/dev/ttyUSBx` or `/dev/ttyACMx`.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Tab. 6: Grinn GenioBoard recommended ratings

	Minimum	Typical	Maximum	Unit
Supply voltage	5.0		20.0	V
Supply current			5	A
Operating ambient temperature	-20	25	70	°C

7 Mechanical Characteristics

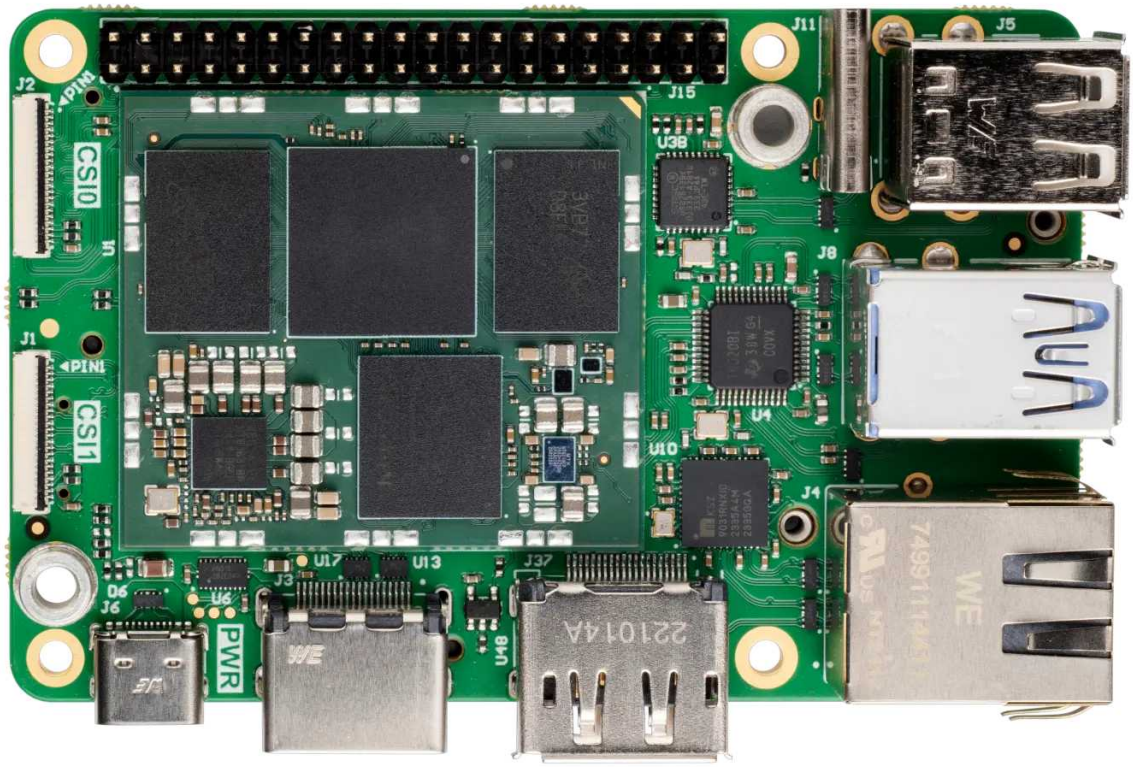


Fig. 15: Grinn GenioBoard top view

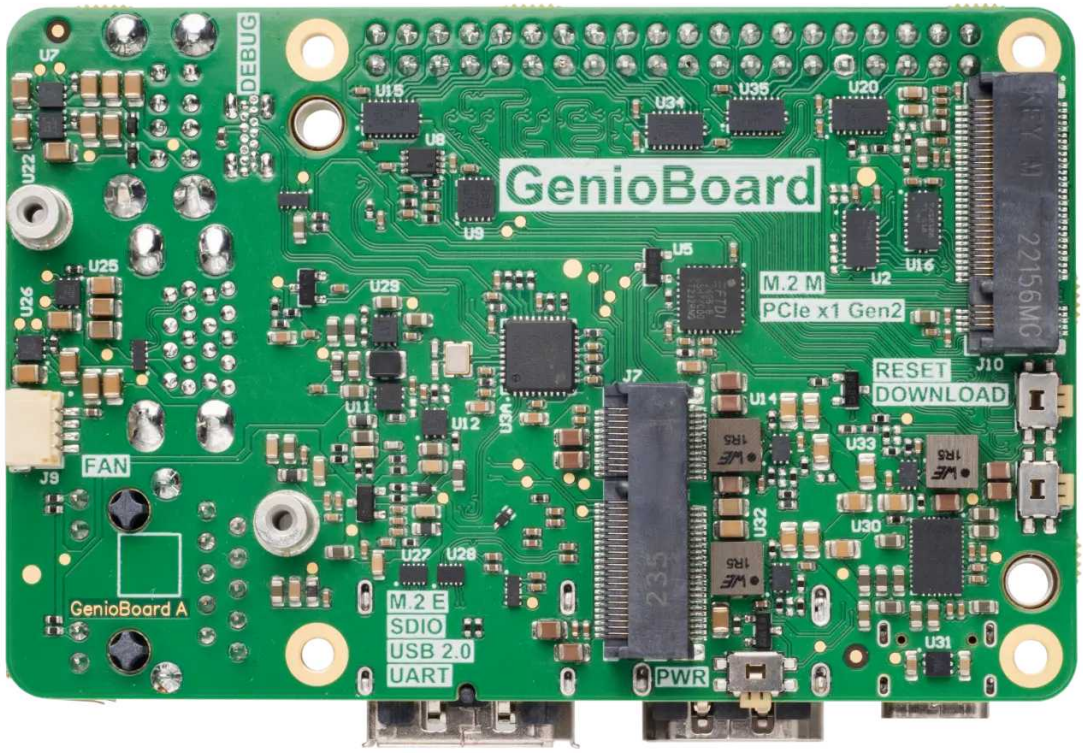


Fig. 16: Grinn GenioBoard bottom view

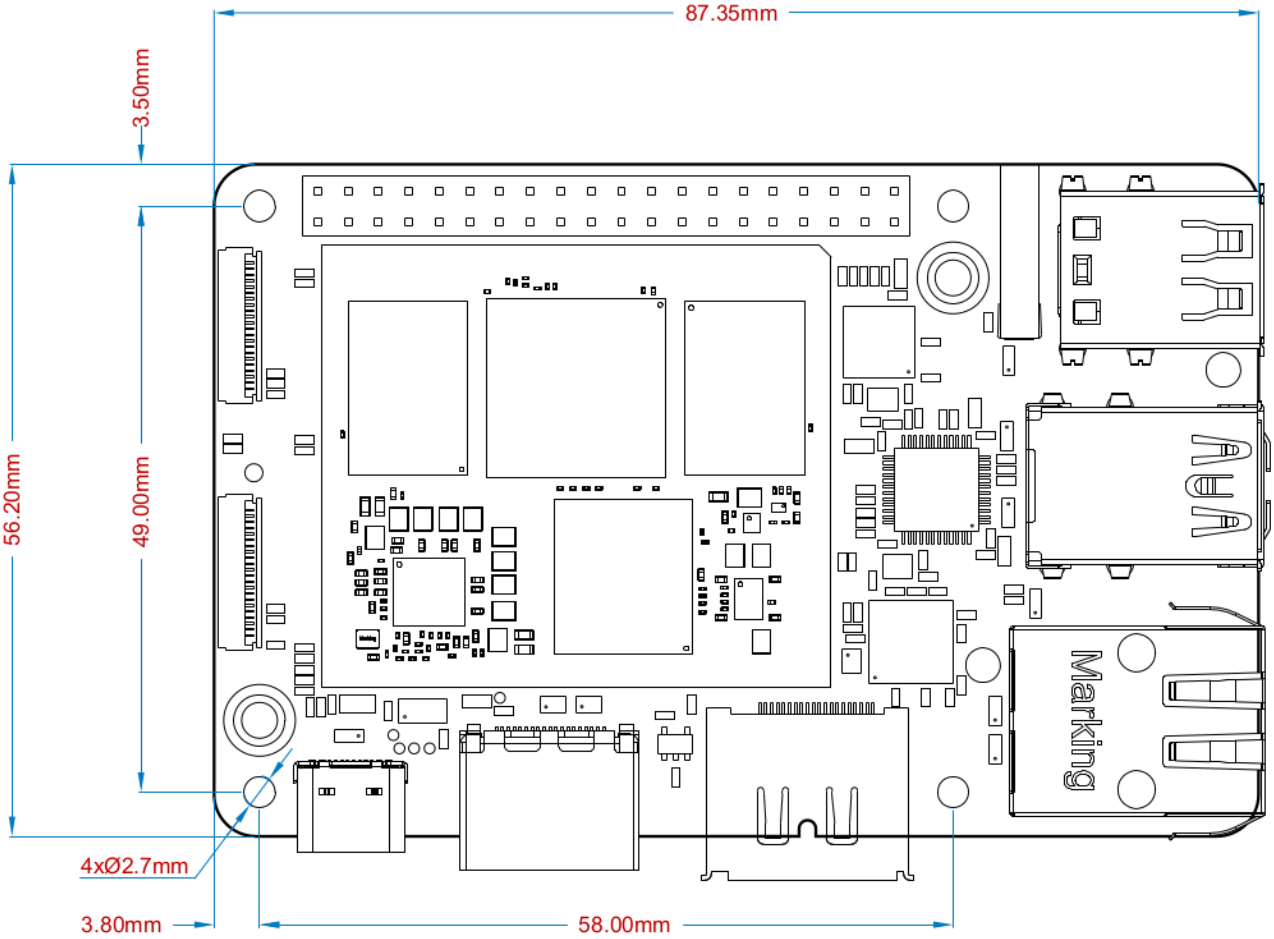


Fig. 17: Grinn GenioBoard top view dimensions

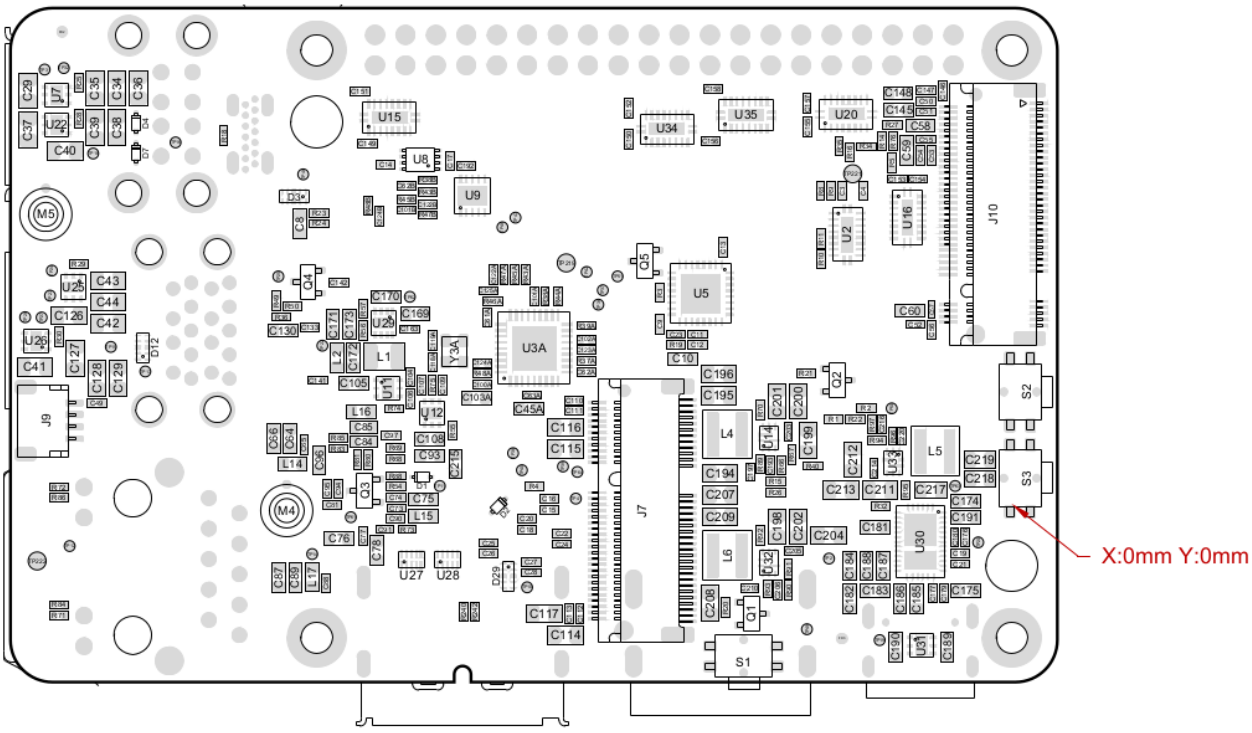
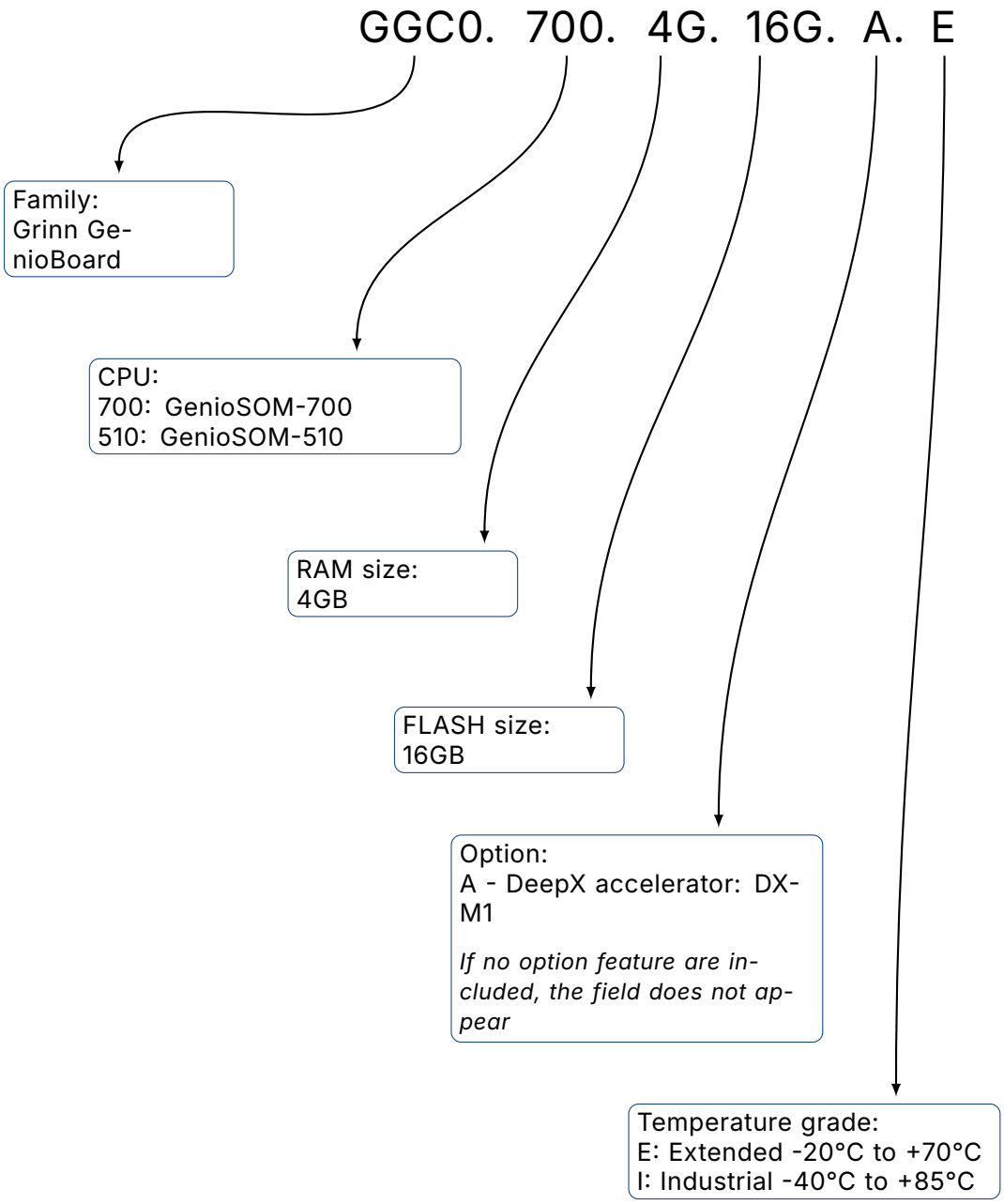
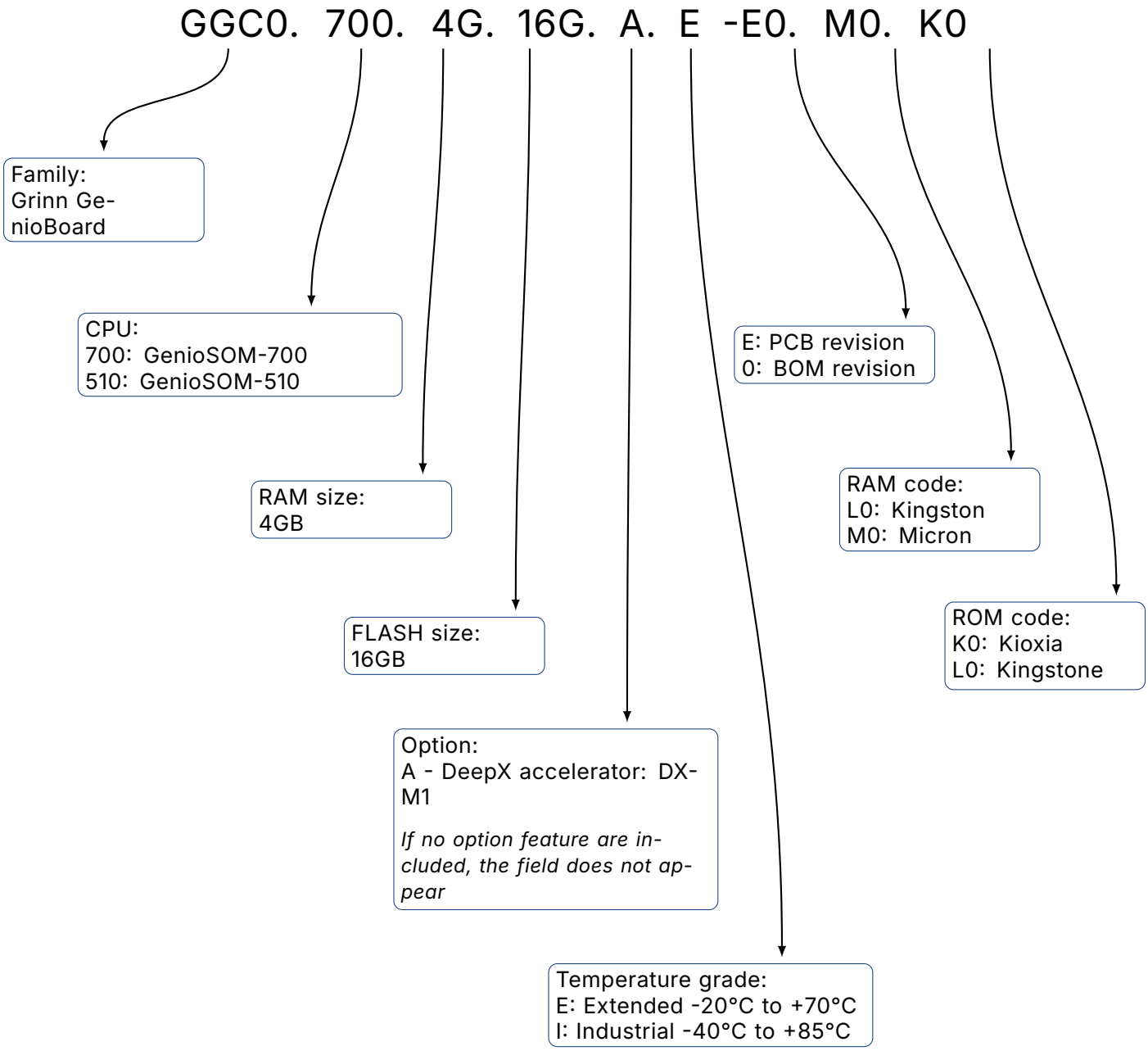


Fig. 18: Grinn GenioBoard bottom view dimensions

8 Ordering Part Number



9 Full Part Number



Revision History

Revision	Date	Description
1.0	2025-06-18	Initial revision.
1.1	2025-07-07	Added PSU diagram.
1.2	2025-07-11	Added alt function in 40-pin header; corrected functional block diagram; added flashing figure; minor fixes.
1.3	2025-07-31	Updated naming convention.
1.4	2025-08-29	Updated 40-pin header table and figure.
1.5	2025-10-30	Added ordering information.
1.6	2025-11-17	Updated to revision B0.
1.7	2025-12-10	Updated chapter 8; added chapter 9; added TXS0108 information.
1.8	2025-12-15	Added Deepx chapter.
1.9	2026-01-14	Minor update in power supply chapter.
2.0	2026-02-19	Minor update in naming convention.
2.2	2026-04-23	Updated PCB revision; new template; added Cabling Guidelines.
2.3	2026-04-30	Updated link in the Flashing section.
2.4	2026-05-25	Updated RAM capacity information.

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