

1 About Grinn EvseSOM™

The Grinn EvseSOM™ is a highly integrated System-on-Module (SOM) designed to serve as the core of a Supply Equipment Communication Controller (SECC) for eMobility applications.

It is driven by an **NXP i.MX RT1061** processor and a **Lumissil IS31CG5317** transceiver, acting as a bridge between the vehicle charging interface and a host application processor.

The module simplifies EVSE design by providing a complete software stack for global charging standards, including **ISO 15118**, **DIN 70121**, and **IEC 61851-1**, while operating from a single 5 V power supply.

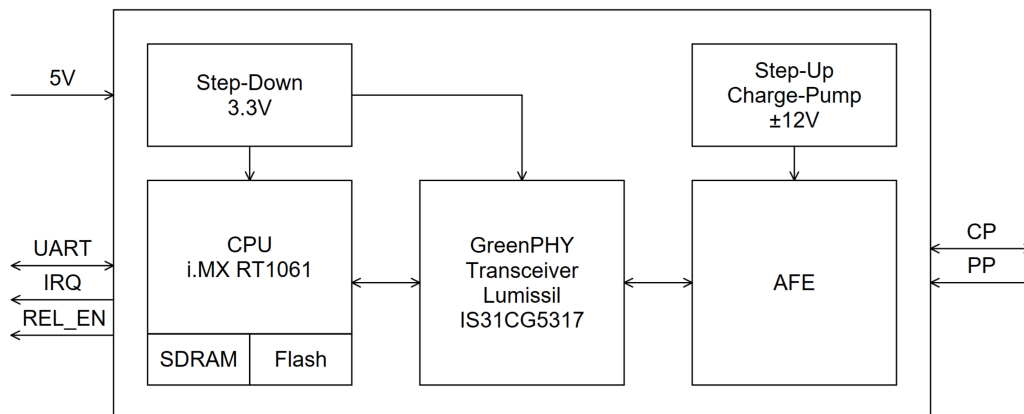
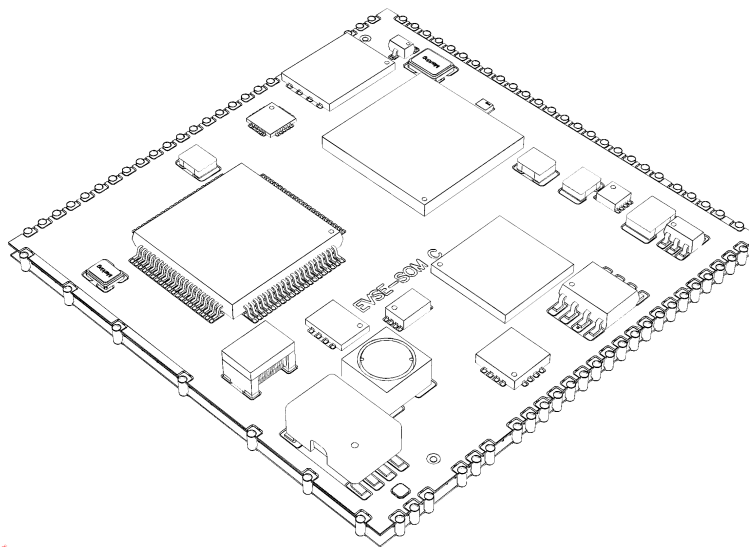


Fig. 1: Grinn EvseSOM™ block diagram

1.1 Document purpose

The purpose of this document is to define minimum requirements for hardware configuration and show how to integrate the Grinn EvseSOM™ ISO 15118-compliant communication module into an EVSE design.



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2 Design requirements

2.1 Power management

The Grinn EvseSOM™ module is designed for single-supply operation, which simplifies the overall carrier board design.

- **Input Voltage:** Requires a single 5 V input (range 4.5 V to 5.5 V).
- **Consumption:** Typically consumes 140 mA to 225 mA (max 1.5 W).
- **Filtering:** Add 10 µF to 22 µF bulk capacitor between the 5 V power rail input (pins 36–37) and GND (pins 34–35).
- **Ground:** Connect all GND pins to the carrier board ground.
- **3.3 V output (optional):** If required, use 3.3 V outputs (pins 14, 15, 62) as an interface voltage reference. Do not connect loads over 50 mA.

2.2 Electric Vehicle interface

The entire physical layer of the connection to the EV is managed by the Grinn EvseSOM™.

- **Control Pilot (CP):** Connect P9 (PILOT) to the charging socket CP pin. The module autonomously handles PWM generation, HLC and feedback voltage sensing.
- **Proximity Pilot (PP):** Connect P11 (PROX) to the charging socket PP pin to monitor cable current capacity and connection state.
- **Grounding:** Connect P10 (PILOT GND) specifically to the charging socket Protective Earth (PE) pin.

Note

Protect CP and PP signals with a proper overvoltage protection component such as a varistor or TVS.
Provide also space for a capacitor between the CP and CP_GND lines, which will help reduce EMI signals if necessary.

2.3 Safety Interlock and High-Voltage Path Control

The safety feature is implemented by controlling the main relay from two separate sources—the Grinn EvseSOM™ and the host processor. This prevents the power supply from being activated in the case of a failure in one of the components.

2.3.1 Hardware Interlock

The module provides a dedicated relay enable (**REL_EN**) signal on pin P31. This is an active-high hardware signal that only transitions to high when the SOM has validated a safe charging state and the absence of CP faults.

2.3.2 Mandatory Boolean Logic

Designer **MUST** implement a hardware-level AND gate on the carrier board. The final relay control must satisfy the following logic:

$$REL_EN = REL_EN_{EvseSOM} \wedge REL_EN_{HOST}$$

This ensures that if the SOM detects a protocol deviation or the Host initiates an emergency stop, the high-voltage path is interrupted within milliseconds, regardless of software resets or MCU hangs.

2.4 Host interface

Communication with the Host Application Processor occurs via a high-speed asynchronous serial interface.

- **UART Physical Layer:** Uses a 2-wire UART (TX, RX) with 3.3 V CMOS logic levels (P42–P45).
- **Asynchronous Signaling (IRQ):** A dedicated IRQ line (P51) is provided. This allows the Grinn EvseSOM™ to signal the host immediately upon status changes (e.g. EV detection or faults) without requiring constant polling.
- **Protocol:** Data exchange follows a Modbus-based protocol where the Grinn EvseSOM™ acts as a slave device.

Note

Add series resistors (1 to 2.2 kOhm) on the carrier board on TX and RX pins to comply with the Grinn EvseSOM™ internal circuit.

2.5 Module reset

Reset input is connected to pin 49. It is an active-low signal with internal pull-up. Drive it low for at least 100 ms to reset the module.

2.6 Safety and security

The hardware architecture enforces a clear division of responsibility for system safety.

- **Negotiation vs. Power Control:** The Grinn EvseSOM™ manages the communication negotiation, but the **host CPU** must maintain ultimate control over the high-voltage power path, including driving power relays or contactors.
- **Secure Boot:** The module implements a secure boot chain, only executing firmware images cryptographically signed with a valid certificate to prevent tampering.
- **In-System Programming (ISP):** Firmware can be upgraded remotely by the host CPU while the Grinn EvseSOM™ is mounted in the finished product.

2.7 Carrier board space constraint

Integrating the Grinn EvseSOM™ requires careful consideration of the physical footprint and mechanical clearances on your carrier board.

- **Physical Footprint:** The module has a compact rectangular footprint of 42.50 mm × 43.50 mm.
- **Module Height:** The total height of the module is 5.25 mm, which must be accounted for when selecting an enclosure or stacking additional PCBs.
- **Pad Geometry:** The module uses castellated pads for soldering. The individual pad dimensions are 0.60 mm in depth from the edge and 1.00 mm in width. Soldering pads on the carrier board should be slightly longer, i.e. 1.5 mm × 1.0 mm, to ensure proper amount of solder paste.
- **Pin Pitch and Alignment:** Pad positioning follows a specific grid defined in the mechanical section of the datasheet.
- **Overall Space:** A minimum area of 45 mm × 46 mm is required on the carrier board to properly install the module.

Note

Ensure that the power supply and all other signals are properly protected on the carrier board against ESD and overcurrent with TVS, varistors, and/or fuses.

3 Schematics

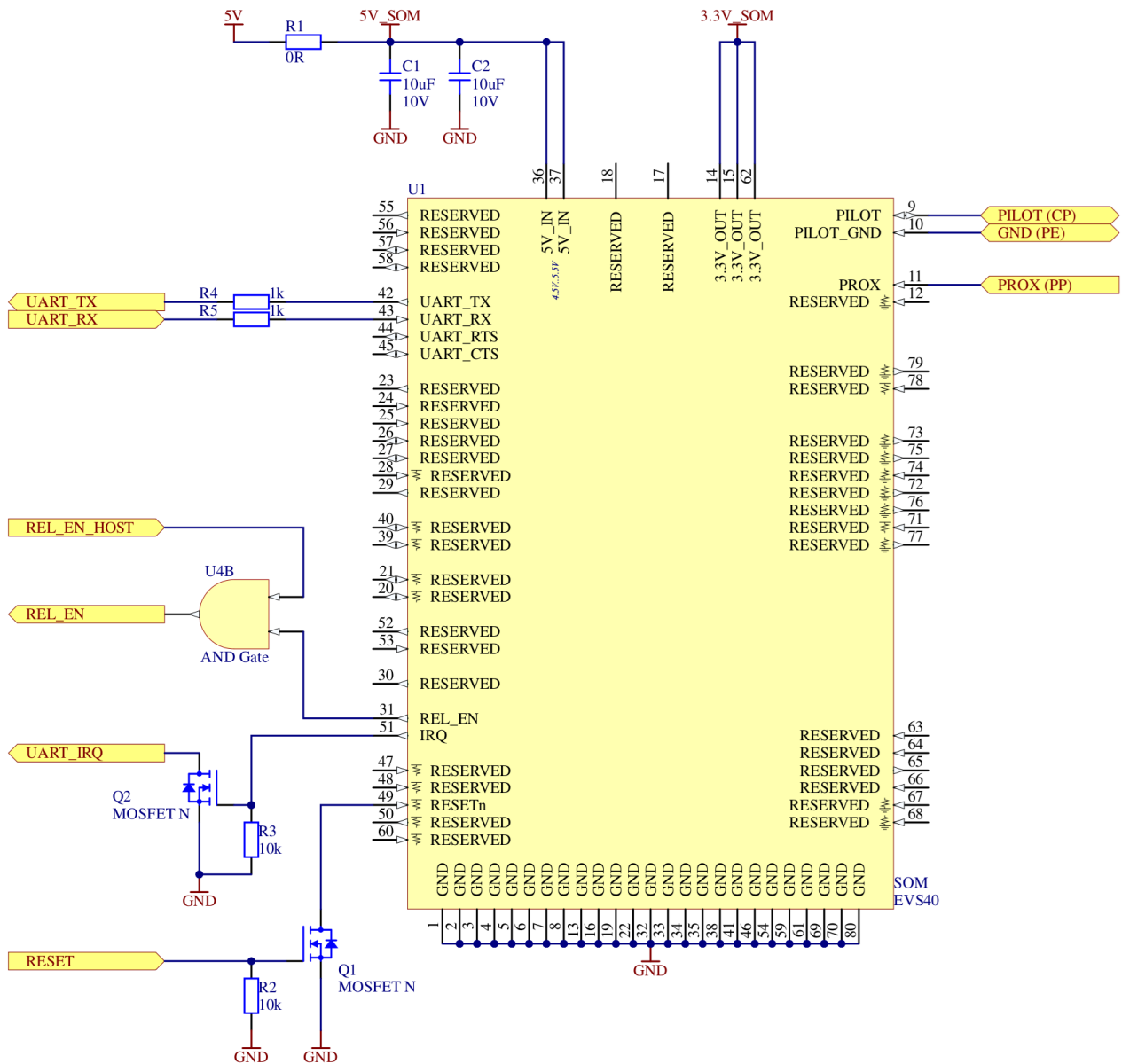


Fig. 2: Grinn EvseSOM™ application example schematic

4 Mechanical Characteristics

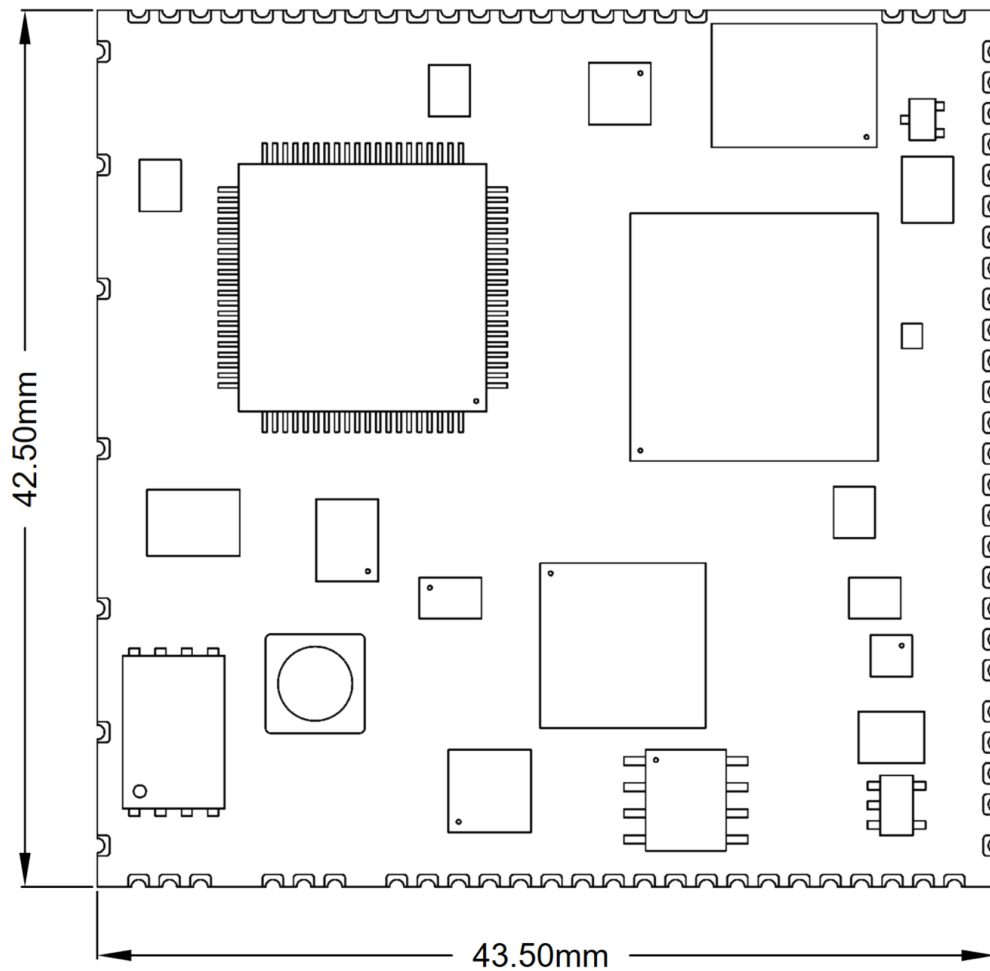


Fig. 3: Grinn EvseSOM™ dimensions

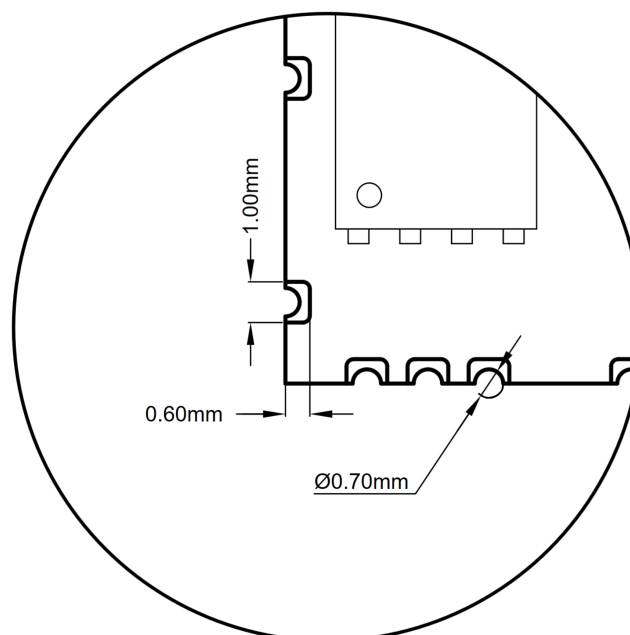


Fig. 4: Grinn EvseSOM™ pad dimensions



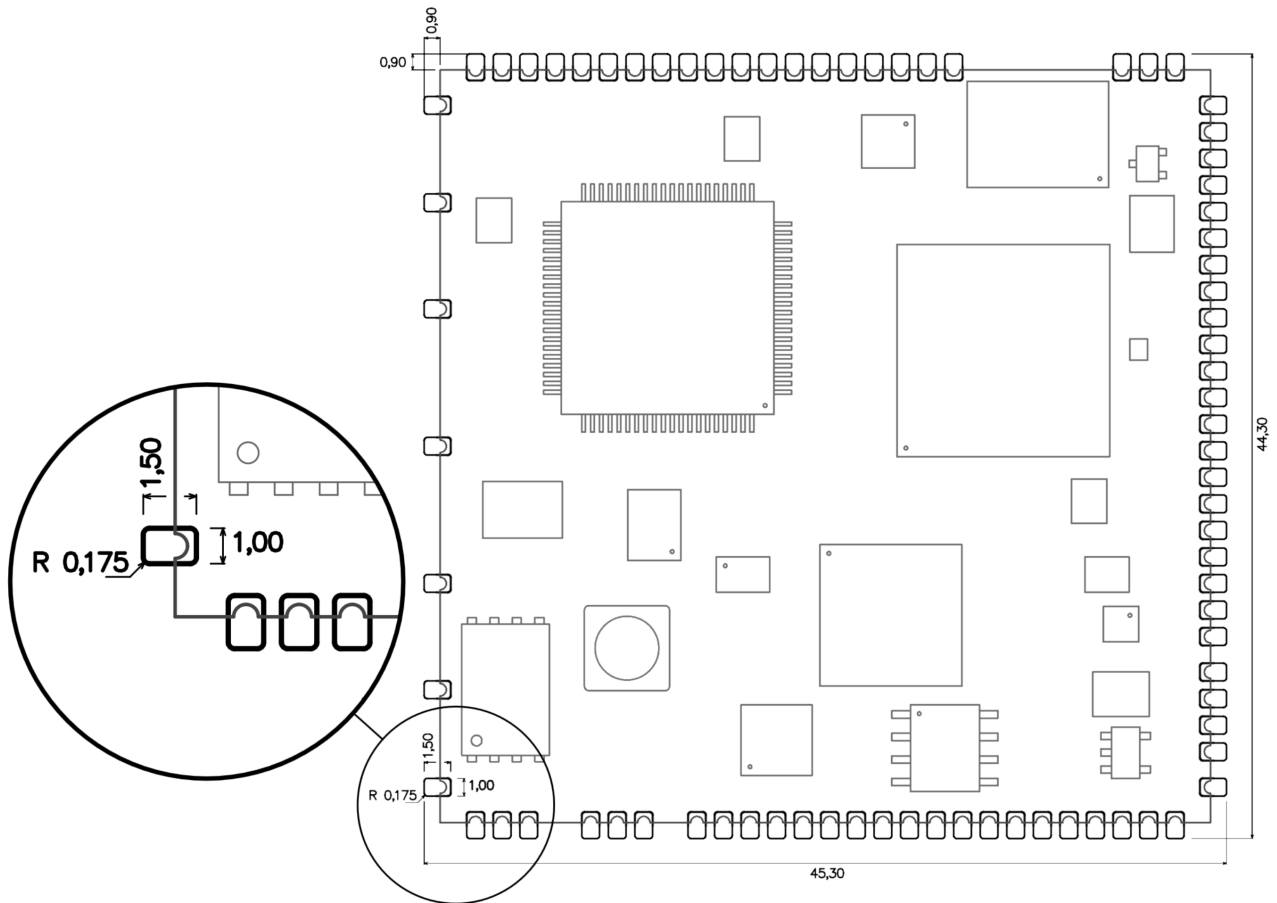


Fig. 6: Grinn EvseSOM™ Footprint example

Revision History

Revision	Date	Description
1.0	2026-09-08	Initial release.



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