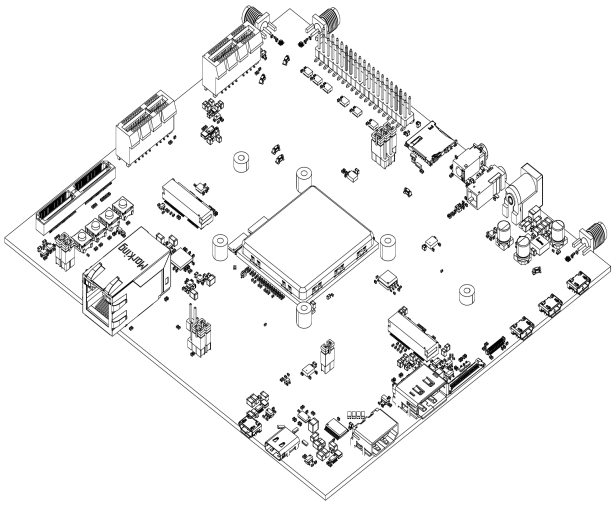
GenioSOM Evaluation Board User Guide



1 Features

- Convenient voltage, current, and signal measurement points
- Accelerated time-to-market
- Integrated on-board debugger
- Programming via a single USB cable
- Single power supply input with a 2.5/5.5mm DC jack
- MicroSD card socket
- Raspberry Pi HAT-compatible interface
- 5G antenna SMA connectors
- eDP, HDMI, and DisplayPort (DP) interfaces
- 10/100/1000 Mbps Ethernet PHY with RGMII interface
- M.2 socket for 5G module
- USB-C port
- Micro USB OTG
- 3x built-in USB to UART interfaces
- 3x MEMS Microphones
- 2x 3.5mm jack
- 1x connector for a custom display module
- 2x DSI connectors with dedicated switch
- 2x CSI-2 camera interfaces
- 2x M.2 connectors for WiFi & Bluetooth modules
- 2x WiFi/Bluetooth antenna connectors

2 Applications

- AI supported computer vision applications
- Advanced IoT devices
- Smart home applications
- Industrial automation
- Streaming audio and video
- Multimedia applications

3 Description

Grinn's GenioEVB is a versatile evaluation platform for the GenioSOM module, designed to accelerate application development and provide seamless access to all key peripherals. With a wide array of dedicated headers, GenioEVB ensures effortless integration of various sensors and modules with GenioSOM. It serves as an ideal reference for customers, streamlining the design of schematics and PCB layouts for new product development.

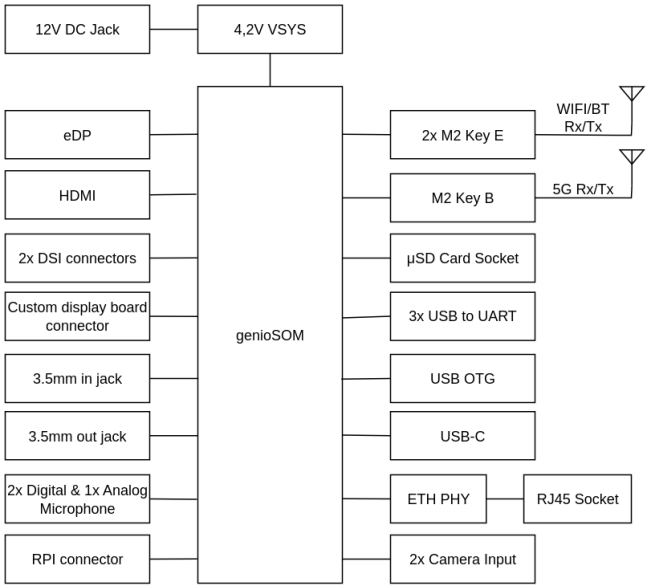


Figure 1: Functional block diagram

Contents

1 Features **1**

2 Applications **1**

3 Description **1**

4 Functional Description **3**
4.1 Power Supply . . . 3
4.1.1 Raspberry Pi HAT . . . 5
4.2 Video Interfaces . . . 7
4.2.1 DP/eDP/HDMI . . . 7
4.2.2 DSI . . . 9
4.2.3 CSI . . . 13
4.3 Audio Interfaces . . . 16
4.4 Wireless Interfaces . . . 18
4.4.1 Wi-Fi and BLE . . . 18
4.4.2 5G . . . 22
4.5 Ethernet . . . 25
4.5.1 Ethernet PHY Resistor Switch . . . 25
4.6 USB . . . 25

5 Boot options **27**
5.1 Supported OS . . . 27
5.2 Flashing . . . 27

6 Electrical Characteristics **28**
6.1 Absolute Maximum Ratings . . . 28

7 Revision History **29**

4 Functional Description

4.1 Power Supply

The GenioEVB power distribution system is engineered for optimal efficiency, ensuring reliable power delivery to various system components while maintaining signal integrity and thermal performance. Powered by a 12V DC input, the system typically requires only 20W for most applications. It incorporates buck converters, linear regulators, and boost converters, all designed to provide efficient and stable power across the platform.

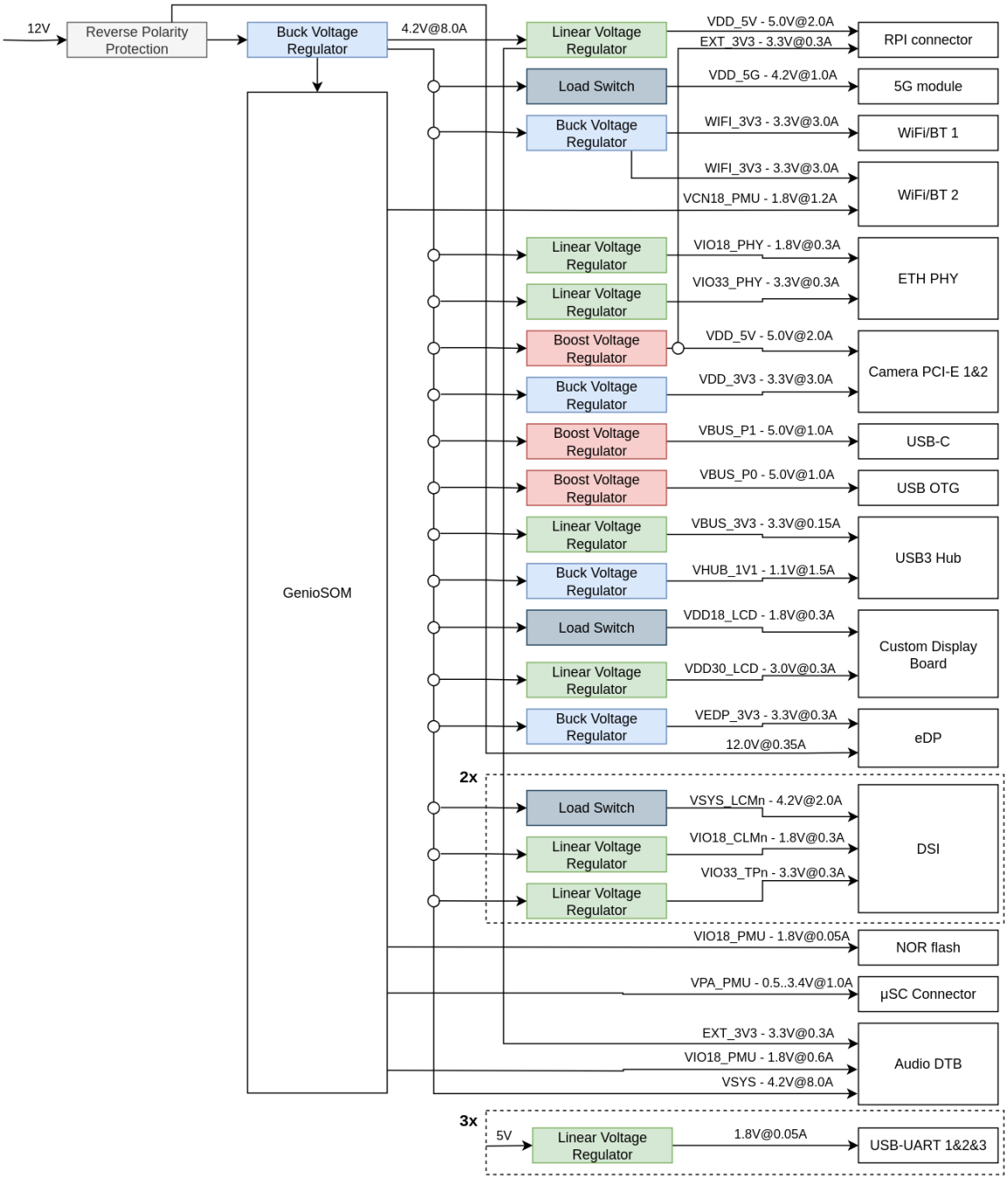


Figure 2: GenioEVB power supply diagram

The table below shows the relationship between each control signal and the domain it controls. Domains not listed are always enabled, ensuring essential functions remain active while others can be dynamically managed when needed.

Table 1: GenioEVB control signals to domains mapping

CPU Pin	Schematic signal	Switchable domains
I2SIN_D1	LCM1_EN	VIO18_LCM1 & VSYS_LCM1
USB2_DRV_VBUS	LCM2_EN	VIO18_LCM2 & VSYS_LCM2
DPI_D14	ETH_TXER	VIO18_PHY
GPIO15	15.6LCM_POWER_EN	VEDP_3V3
SPI0_MIO3	WIFI_3V3_EN	WIFI_3V3
USB2_VBUS_VALID	CAMERA_3V3_EN	VDD_3V3
I2SO2_D2	LCM1_TP_EN	VIO33_TP1
I2SO2_D3	LCM2_TP_EN	VIO33_TP2
I2SIN_D2	HUB_3V3_EN	VHUB_3V3
DPI_D15	ETH_RXER	VIO33_PHY
GPIO09	GPIO_3V3_EN	EXT_3V3
GPIO10	5V_EN	VDD_5V

4.1.1 Raspberry Pi HAT

The GenioSOM supports the Raspberry Pi HAT connector, as shown in the schematic below. To route the RPI_UART signal, reconfigure the J17 and J18 goldpin jumpers. All pins are 3.3V compatible, ensuring seamless integration with Raspberry Pi accessories.

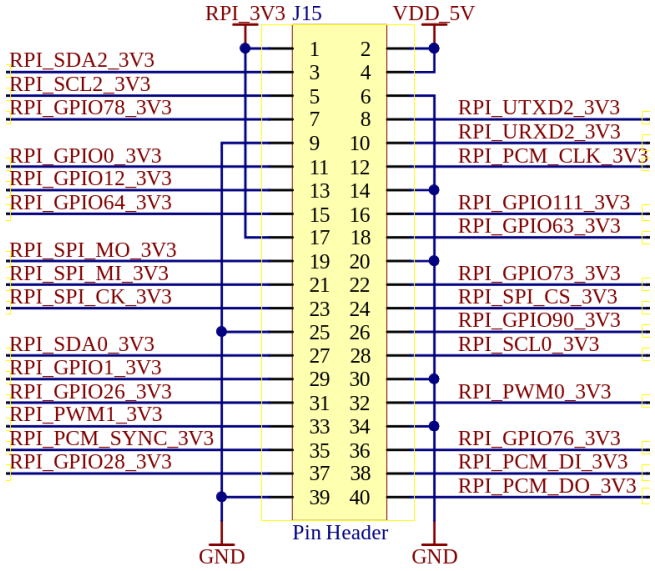


Figure 3: Raspberry Pi HAT connector schematic

Table 3: Raspberry Pi HAT connector pinout

Pin	Signal
1	3.3V
2	5V
3	I2C2_SDA
4	5V
5	I2C2_SCL
6	GND
7	GPIO78
8	RPI_UART_TXD
9	GND
10	RPI_UART_RXD
11	GPIO0
12	PCM_CLK
13	GPIO12
14	GND
15	GPIO64
16	GPIO111
17	3.3V
18	GPIO63
19	SPI2_MOSI
20	GND
21	SPI2_MISO
22	GPIO 25
23	SPI2_SCLK
24	SPI2_CS
25	GND
26	GPIO90
27	I2C0_SDA

Pin	Signal
28	I2C0_SCL
29	GPIO1
30	GND
31	GPIO26
32	PWM0
33	PWM1
34	GND
35	PCM_SYNC
36	GPIO76
37	GPIO28
38	PCM_DI
39	GND
40	PCM_DO

4.2 Video Interfaces

4.2.1 DP/eDP/HDMI

The GenioEVB features an HDMI receptacle, a DisplayPort HDMI receptacle, and a 30-pin wire-to-board female eDP connector, providing versatile display connectivity options.

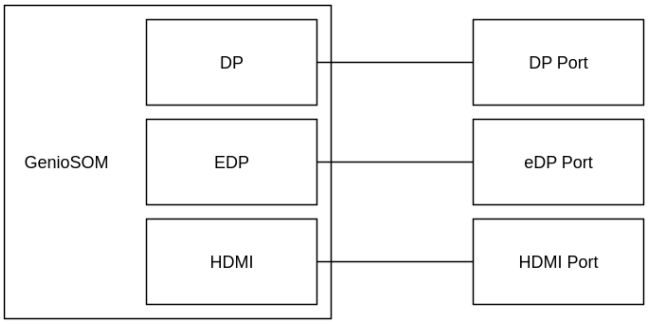


Figure 4: GenioEVB display connectivity diagram

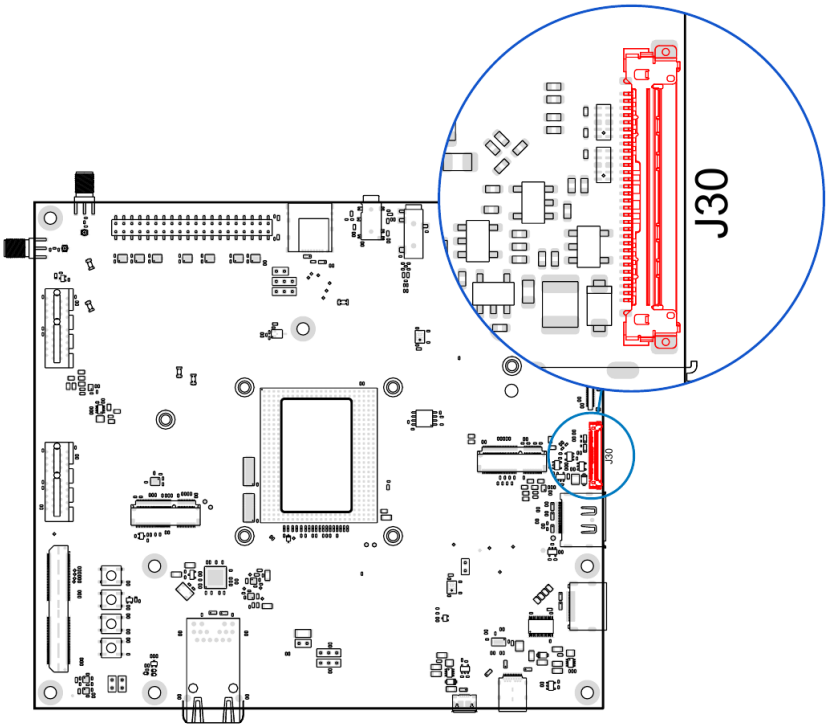


Figure 5: GenioEVB eDP connector

Table 5: GenioEVB eDP pinout

Pin	Signal
2	12V_DC
3	12V_DC
4	12V_DC
5	12V_DC
6	NC
7	NC
8	DISP_PWM0
9	DISP_EN
10	GND
11	GND
12	GND
13	GND
14	EDP_HPD
15	GND
16	GND
17	NC
18	VEDP_3V3
19	VEDP_3V4
20	GND
21	EDP_AUX_N
22	EDP_AUX_P
23	GND
24	EDP_LN0_TX_P
25	EDP_LN0_TX_N
26	GND
27	EDP_LN1_TX_P
28	EDP_LN1_TX_N
29	GND
30	NC

4.2.2 DSI

The GenioEVB offers three connectors with a switch to select between the Custom Display Board Connector (CDBC), DSI0, and DSI1 interfaces. The CDBC provides flexibility in configuration: it can enable both DSI0 and DSI1 interfaces simultaneously. In contrast, the DSI0 Connector is exclusively compatible with the DSI0 interface, while the DSI1 Connector can only connect to the DSI1 interface.

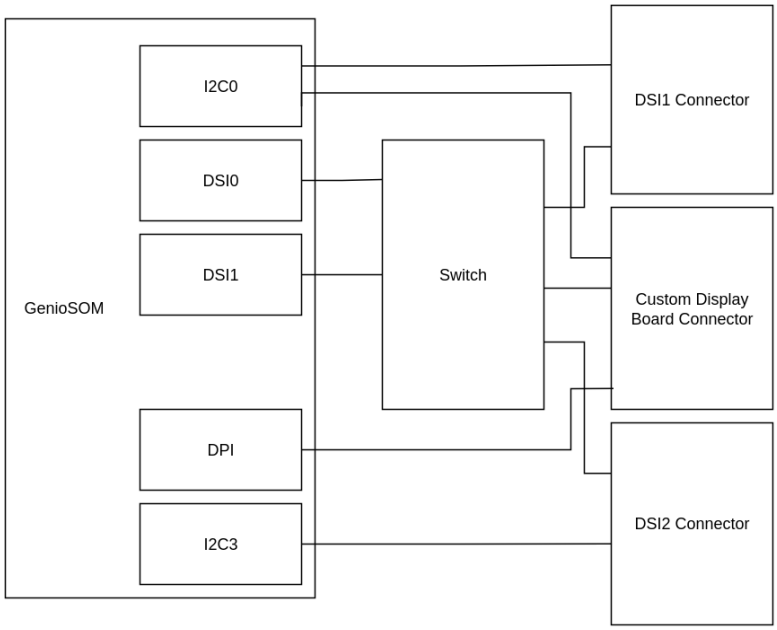


Figure 6: GenioEVB DSI diagram

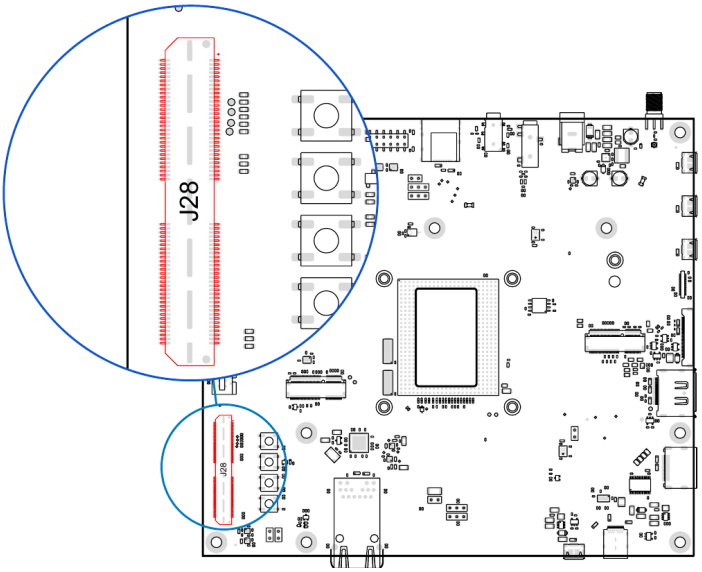


Figure 7: GenioEVB Custom Display Board Connector

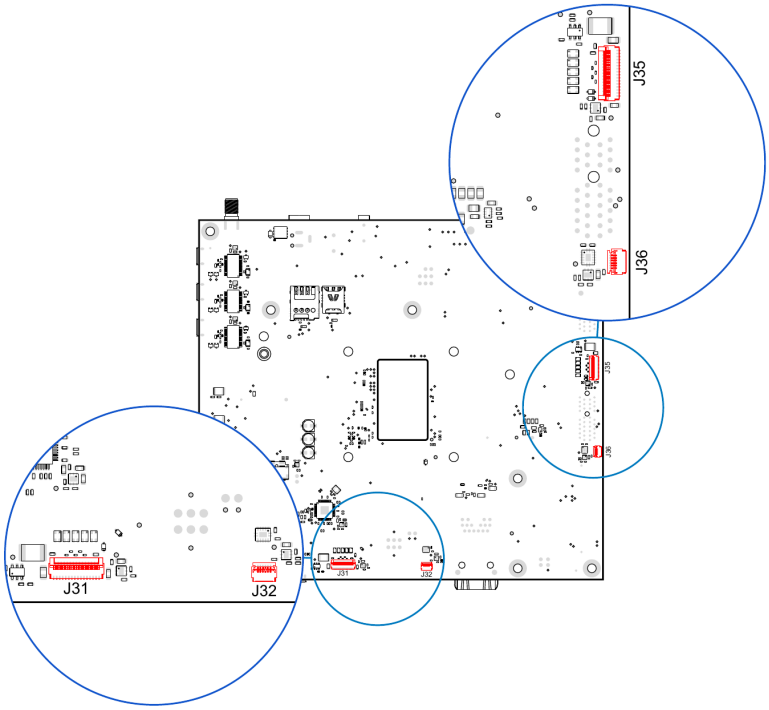


Figure 8: GenioEVB DSI connectors

Table 7: GenioEVB DSI1 pinout

Pin	Signal DSI1	Signal DSI2
1	VIO18_CLM1	VSYS
2	LCM1_BL_EN	VSYS
3	GND	VSYS
4	GND	VSYS
5	VSYS	GND
6	VSYS	LCM2_BL_EN
7	NC	NC
8	DSI0_LCM_RST	GND
9	GND	DSI1_D3_N
10	DSI0_D2_P	DSI1_D3_P
11	DSI0_D2_N	GND
12	GND	DSI1_D0_N
13	DSI0_D1_P	DSI1_D0_P
14	DSI0_D1_N	GND
15	GND	DSI1_CK_N
16	DSI0_CK_P	DSI1_CK_P
17	DSI0_CK_N	GND
18	GND	DSI1_D1_N
19	DSI0_D0_P	DSI1_D1_P
20	DSI0_D0_N	GND
21	GND	DSI1_D2_N
22	DSI0_D3_P	DSI1_D2_P
23	DSI0_D3_N	GND
24	GND	DSI0_LCM_RST
25	NC	NC
26	LCM1_BL_EN	VSYS
27	GND	VSYS
28	VSYS	GND
29	VSYS	GND
30	VSYS	LCM2_BL_EN
31	VSYS	VIO18_CLM1

Table 9: GenioEVB DSI1 pinout

Pin	Signal DSI1	Signal DSI2
1	GND	VIO33_TP
2	I2C0_SDA0_3v3	GPIO_CTP0_RST_3V3
3	I2C0_SCL0_3v3	ENIT_CTP0_INT_3V3
4	ENIT_CTP0_INT_3V3	I2C3_SCL3_3v3
5	GPIO_CTP0_RST_3V3	I2C3_SDA3_3v3
6	VIO33_TP1	GND

To expose the DPI interface to the Custom Display Board Connector default resistor switch configuration has to be changed as described in 4.5.1

Table 11: GenioEVB Custom Display Board Connector pinout

Pin	Signal	Pin	Signal
2	GND	62	NC
3	NC	63	NC
4	DSI0_CK_P	64	NC
5	NC	65	NC
6	DSI0_CK_N	66	NC
7	NC	67	DSI1_CK_P
8	DSI0_D0_P	68	NC
9	NC	69	DSI1_CK_N
10	DSI0_D0_N	70	NC
11	NC	71	DSI1_D0_P
12	DSI0_D1_P	72	DPI_D15
13	NC	73	DSI1_D0_N
14	DSI0_D1_N	74	DPI_D14
15	NC	75	DSI1_D1_P
16	DSI0_D2_P	76	DPI_D13
17	NC	77	DSI1_D1_N
18	DSI0_D2_N	78	DPI_D12
19	NC	79	DSI1_D2_P
20	DSI0_D3_P	80	DPI_D11
21	NC	81	DSI1_D2_N
22	DSI0_D3_N	82	DPI_D10
23	NC	83	DSI1_D3_P
24	NC	84	DPI_D9
25	CTP_SCL_DTB	85	DSI1_D3_N
26	NC	86	DPI_D8
27	CTP_SDA_DTB	87	NC
28	NC	88	NC
29	CTP_EINT_DTB	89	NC
30	NC	90	NC
31	DSI1_TE_DTB	91	NC
32	NC	92	DPI_D7
33	DSI0_TE_DTB	93	NC
34	NC	94	DPI_D6
35	GND	95	NC
36	DPI_VSYNC	96	DPI_D5
37	NC	97	NC
38	NCDPI_HSYNC	98	DPI_D4
39	GND	99	NC
40	DPI_DE	100	DPI_D3
41	NC	101	NC
42	NC	102	DPI_D2
43	NC	103	NC
44	DPI_CK	104	DPI_D1
45	NC	105	NC
46	NC	106	DPI_D0
47	NC	107	NC
48	NC	108	VDD30_LCD

Pin	Signal	Pin	Signal
49	LCM0_RST_DTB	109	VSYS
50	NC	110	VDD30_LCD
51	CTP_RSTn_DTB	111	NC
52	NC	112	VDD30_LCD
53	LCM1_RST_DTB	113	NC
54	NC	114	VDD18_LCD
55	NC	115	DISP_PWM1_DTB
56	NC	116	VDD18_LCD
57	NC	117	DISP_PWM0_DTB
58	NC	118	VDD18_LCD
59	NC	119	LCM_BIAS_EN_DTB
60	NC	120	NC

4.2.3 CSI

The GenioEVB board includes two 4-lane CSI interfaces, each capable of supporting a maximum bit rate of 1.5 Gbps per lane. Camera sub-boards connect to the board using the Molex 777159006 connector.

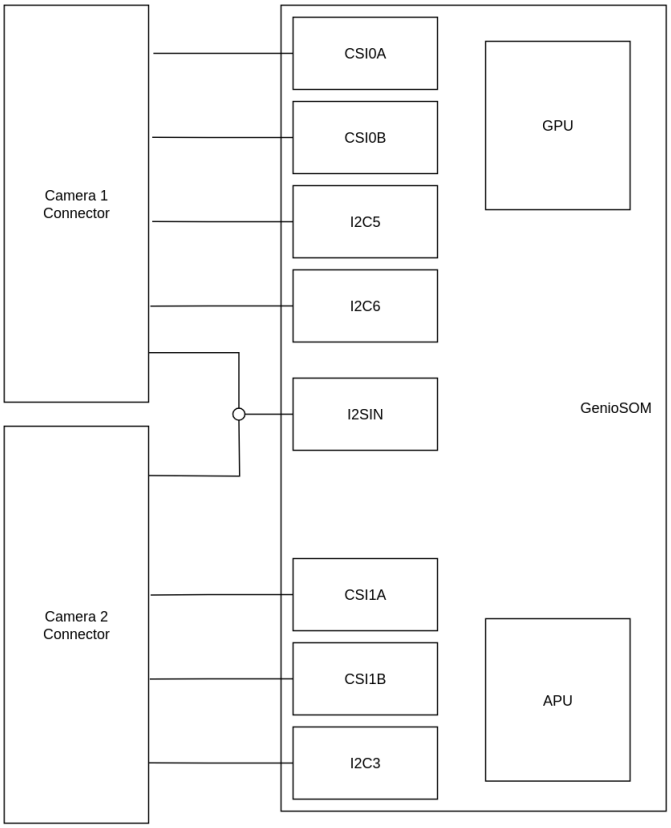


Figure 9: GenioEVB CSI diagram

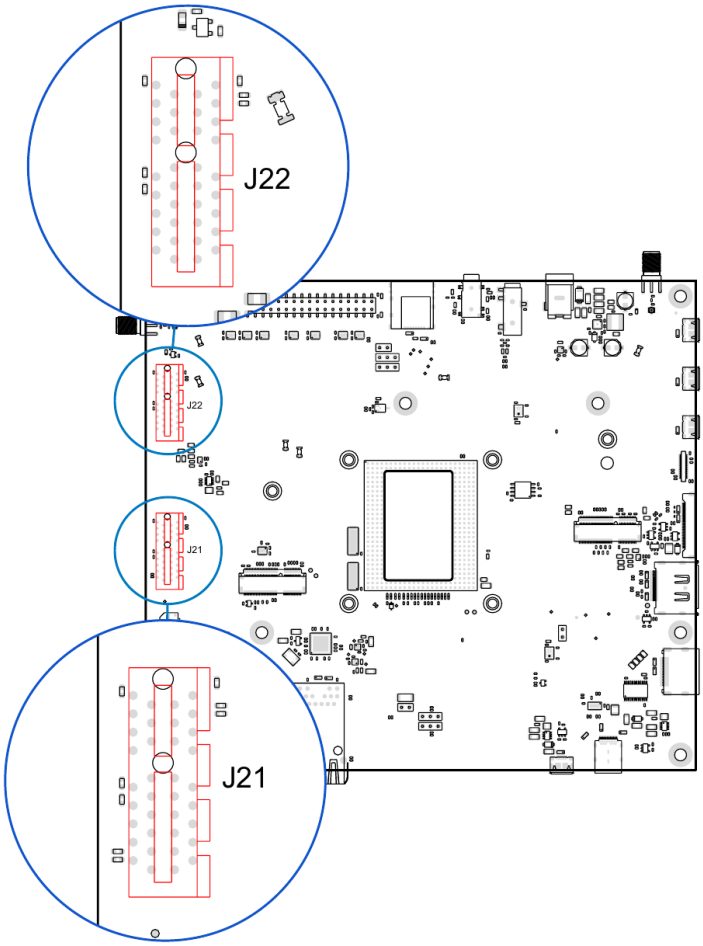


Figure 10: GenioEVB CSI camera connectors

Table 13: GenioEVB CSI camera connectors

Pin	Camera 1 Signal	Camera 2 Signal
B1	GND	GND
B2	CSI0B_L2_N	NC
B3	CSI0B_L2_P	NC
B4	CSI0B_L1_N	CSI1B_L1_N
B5	CSI0B_L1_P	CSI1B_L1_P
B6	CSI0B_L0_N	CSI1B_L0_N
B7	CSI0B_L0_P	CSI1B_L0_P
B8	GND	GND
B9	CSI0A_L2_N	CSI1A_L2_N
B10	CSI0A_L2_P	CSI1A_L2_P
B11	CSI0A_L1_N	CSI1A_L1_N
B12	CSI0A_L1_P	CSI1A_L1_P
B13	CSI0A_L0_N	CSI1A_L0_N
B14	CSI0A_L0_P	CSI1A_L0_P
B15	GND	GND
B16	I2C5_SCL	I2C3_SCL
B17	I2C5_SDA	I2C3_SDA
B18	VDD_5V	VDD_5V
A1	GND	GND

Pin	Camera 1 Signal	Camera 2 Signal
A2	I2C6_SCL	NC
A3	I2C6_SDA	NC
A4	CAM0_AVDD28_EN	CAM0_AVDD28_-EN
A5	CAM1_DVDD_EN	CAM1_DVDD_EN
A6	CAM1_AVDD28_EN	CAM1_AVDD28_-EN
A7	CAM0_DVDD_EN	CAM0_DVDD_EN
A8	CMMRST0	CMMRST1
A9	GND	GND
A10	CMMCLK0	CMMCLK1
A11	GND	GND
A12	CMMPDN0	CMMPDN1
A13	I2SIN_BCK	I2SIN_BCK
A14	I2SIN_MCK	I2SIN_MCK
A15	I2SIN_WS	I2SIN_WS
A16	I2SIN_D0	I2SIN_D0
A17	VDD_3V3	VDD_3V3
A18	VDD_3V4	VDD_3V3

4.3 Audio Interfaces

The user can utilize analog audio through standard CTIA 3.5mm jack connectors, such as a line-in for recording sound or a line-out for transmitting audio signals to other devices. The board features three microphones: two accessible via DMIC interfaces and a third connected to a PMIC, which serves as an analog frontend. Moreover, a single board-to-board connector is available for the user, with its pinout detailed below.

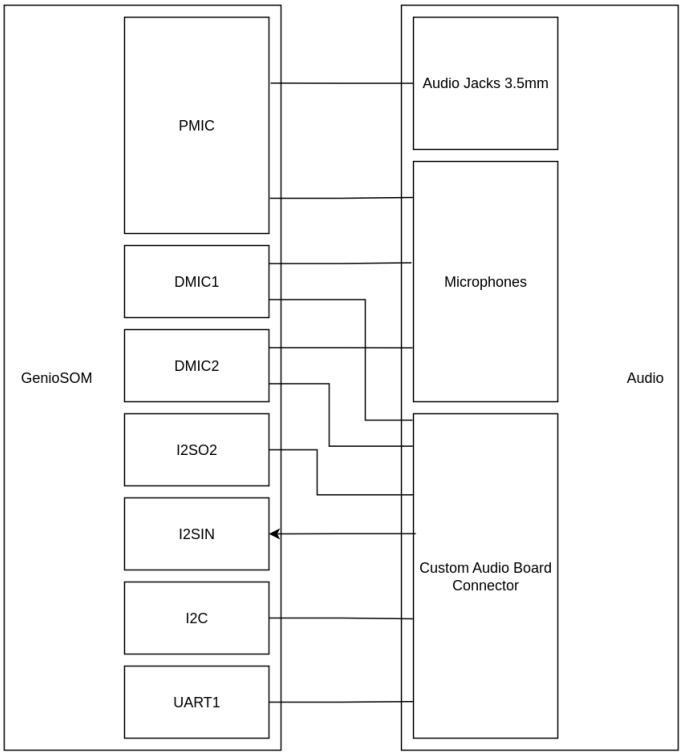


Figure 11: GenioEVB audio diagram

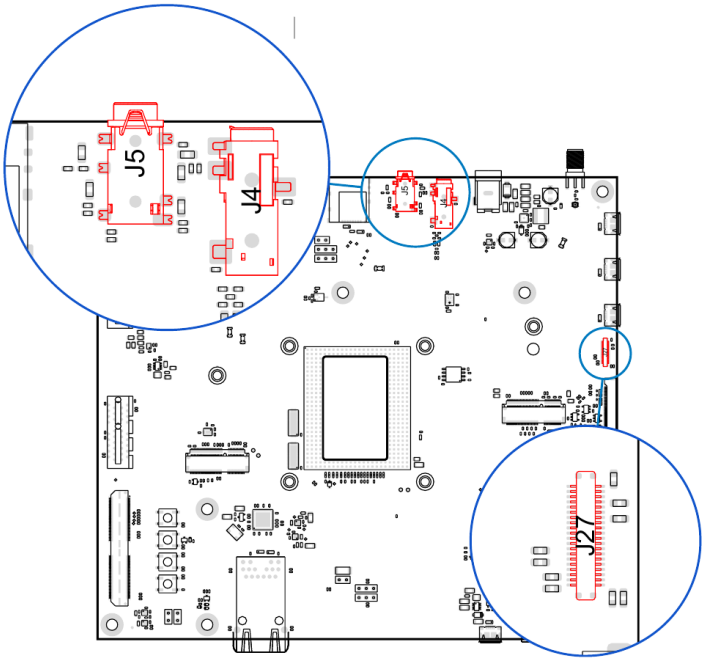


Figure 12: GenioEVB audio connectors

Table 15: GenioEVB custom board-to-board audio connector pinout

Pin	Signal	Testpoint
1	VSYS	-
2	I2C2_SCL	TP93
3	VSYS	-
4	I2C2_SDA	TP94
5	GND	-
6	GND	-
7	EXT_3V3	-
8	I2SIN_MCK	TP95
9	EXT_3V3	-
10	I2SIN_BCK	TP96
11	GND	-
12	I2SIN_WS	TP97
13	VIO18_PMU	-
14	I2SIN_D0	TP98
15	VIO18_PMU	-
16	GND	-
17	GND	-
18	DMIC1_CLK	TP99
19	I2S02_MCK	TP100
20	DMIC1_DAT	TP101
21	I2S02_BCK	TP102
22	GND	-
23	I2S02_WS	TP103
24	DMIC2_CLK	TP104
25	I2S02_D0	TP105
26	DMIC2_DAT	TP106
27	I2S02_D1	TP107
28	GND	-
29	I2S02_D2	TP108
30	BT2_WO	-
31	I2S02_D3	TP117
32	WIFI2_INTn	-
33	GND	-
34	GND	-
35	UART1_TXD	-
36	WIFI1_BT_DISABLE	-
37	UART1_RXD	-
38	EXT_VMCH_EN	-
39	GND	-
40	GND	-

4.4 Wireless Interfaces

Three M.2 connectors are available for the user: two dedicated for Wi-Fi/BLE modules and one for 5G modules. Supported modules include, but are not limited to:

- AzureWave AW-XB468NF (WIFI/BLE)
- Quectel RM500K-CN (5G)

4.4.1 Wi-Fi and BLE

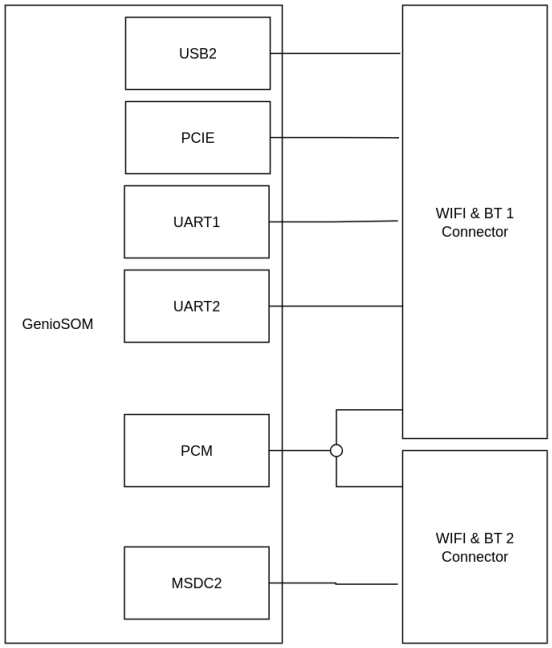


Figure 13: GenioEVB Wi-Fi and BLE diagram

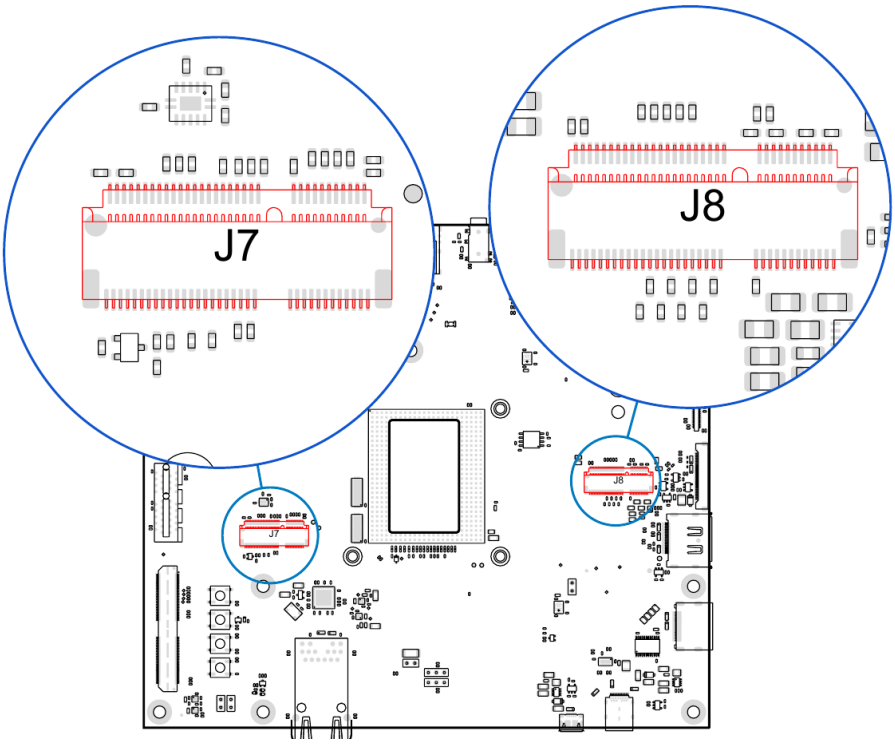


Figure 14: GenioEVB Wi-Fi/BLE connectors

Table 17: GenioEVB Wi-Fi/BLE M.2 Key E slot pinout

Pin	Pin name	Description
1	GND	
2	3.3V	
3	USB2_DP	
4	3.3V	
5	USB2_DN	
6	NC	Connected to TP41
7	GND	
8	NC	R96 to PCM_CLK
9	NC	
10	NC	R97 to PCM_SYNC
11	NC	
12	NC	R98 to PCM_DO
13	NC	
14	NC	R100 to PCM_DO
15	NC	
16	NC	Connected to TP30
17	NC	
18	GND	
19	NC	
20	NC	
21	NC	
22	NC	R103 to UART1_TXD
23	NC	
24-31	Key E	Substrate removed to act as physical key
32	NC	R102 to UART1_RXD
33	GND	
34	NC	R105 to UART2_TXD
35	PCIE_TX0+	
36	NC	R104 to UART2_RXD
37	PCIE_TX0-	
38	NC	
39	GND	
40	NC	
41	PCIE_RX0+	
42	NC	R106 to SPDIF_OUT
43	PCIE_RX0-	
44	NC	
45	GND	
46	NC	
47	PCIE_REFCLK+	
48	NC	
49	PCIE_REFCLK-	
50	NC	Connected to TP3
51	GND	
52	WIFI_PERESETn_3V3	
53	WIFI1_CLKREQ0_3V3	
54	WIFI1_BT_DISABLEn_-3V3	
55	WIFI1_PWAKEn_3V3	

Pin	Pin name	Description
56	WIFI1_WF_DISABLEn_-3V3	
57	GND	
58	NC	
59	NC	
60	NC	
61	NC	
62	NC	
63	GND	
64	NC	
65	NC	
66	NC	
67	NC	
68	NC	
69	GND	
70	NC	
71	NC	
72	3.3V	
73	NC	
74	3.3V	
75	GND	
76	GND	

Table 19: GenioEVB Wi-Fi/BLE M.2 Key E slot pinout

Pin	Pin name
1	GND
2	3.3V
3	NC
4	3.3V
5	NC
6	NC
7	GND
8	NC
9	NC
10	NC
11	NC
12	NC
13	NC
14	NC
15	NC
16	NC
17	NC
18	GND
19	NC
20	NC
21	NC
22	NC
23	SDIO_DS
24-31	Key E
32	NC
33	GND

Pin	Pin name
34	NC
35	MSDC_DATA1
36	NC
37	MSDC_DATA0
38	NC
39	GND
40	NC
41	MSDC_CLK
42	NC
43	MSDC_CMD
44	PCM_DO
45	GND
46	PCM_DI
47	MSDC_DATA3
48	PCM_CLK
49	MSDC_DATA2
50	PCM_SYNC
51	GND
52	WIFI2_RESETn
53	BT2_WO
54	NC
55	WIFI2_INTn
56	NC
57	GND
58	NC
59	NC
60	NC
61	NC
62	NC
63	GND
64	NC
65	NC
66	NC
67	NC
68	NC
69	GND
70	NC
71	NC
72	3.3V
73	NC
74	3.3V
75	GND
76	GND

4.4.2 5G

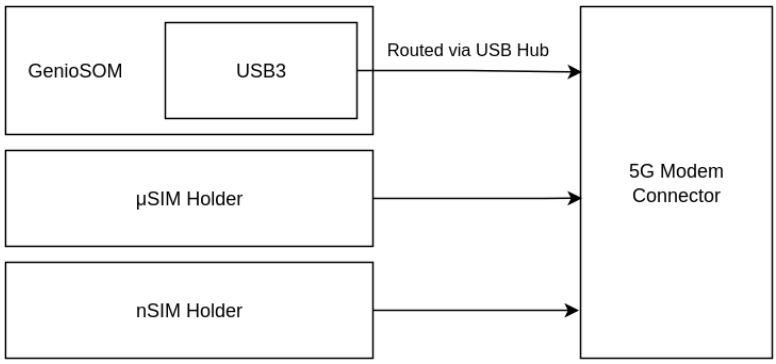


Figure 15: GenioEVB 5G module diagram

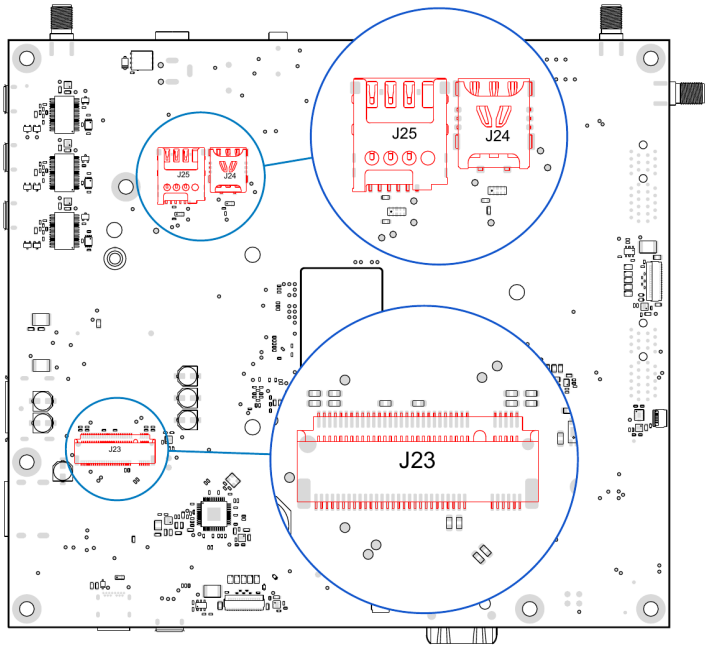


Figure 16: GenioEVB 5G module connectors

Table 21: GenioEVB 5G M.2 Key B slot pinout

Pin	Pin name	Description
1	NC	
2	3.3 V	
3	GND	
4	3.3 V	
5	GND	
6	POWER_ON_OFFn_5G	
7	USB3_DP	
8	NC	Connected to TP224
9	USB3_DN	
10	NC	Connected to TP223
11	GND	
12-19	removed	
20	NC	
21	NC	
22	NC	
23	WAKE_ON_WANn	
24	NC	
25	NC	R231 to GND
26	NC	
27	GND	
28	NC	
29	USB3_TX_N	
30	SIM1_RST	
31	USB3_TX_P	
32	SIM1_CLK	
33	GND	
34	SIM1_DATA	
35	USB3_RX_N	
36	NC	
37	USB3_RX_P	
38	NC	
39	GND	
40	NC	Connected to TP70
41	NC	
42	SIM2_DATA	
43	NC	
44	SIM2_CLK	
45	GND	
46	SIM2_RST	
47	USB3_RX_P	
48	NC	
49	NC	
50	NC	
51	GND	
52	NC	
53	NC	
54	NC	
55	NC	
56	NC	
57	GND	

Pin	Pin name	Description
58	NC	
59	NC	
60	NC	
61	NC	
62	NC	
63	NC	
64	NC	
65	NC	
66	NC	Connected to TP55
67	RESETn_5G	
68	NC	
69	NC	
70	3.3V / VBAT	
71	GND	
72	3.3V / VBAT	
73	GND	
74	3.3V / VBAT	
75	NC	

4.5 Ethernet

The GenioEVB includes an onboard 10/100/1G Ethernet transceiver, the Microchip KSZ9031RNXI. The Ethernet PHY interfaces with the GenioSOM via an RGMII interface.

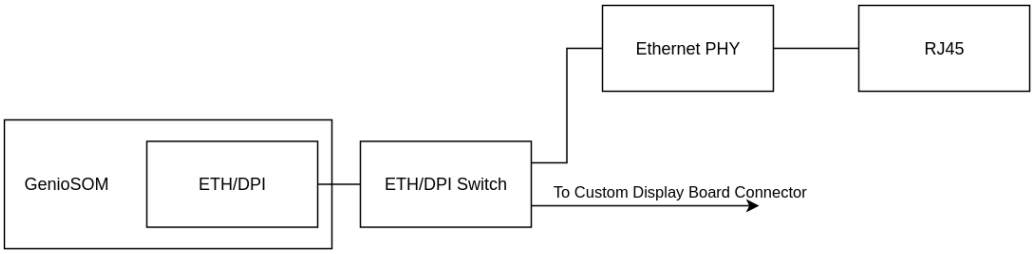


Figure 17: GenioEVB Ethernet diagram

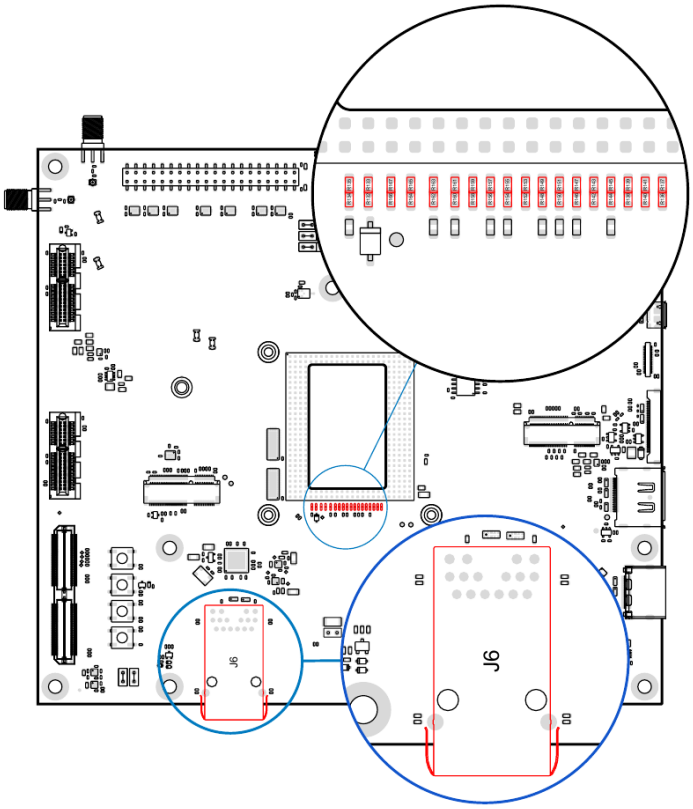


Figure 18: GenioEVB ETH/DPI resistor switch placement and Ethernet connector

4.5.1 Ethernet PHY Resistor Switch

In the default configuration, the resistor switch is set for Ethernet, with jumpers soldered to the even-numbered positions, ranging from R132 to R166. To configure the DPI interface for connection to the display board, the jumpers must be moved to the odd-numbered positions. For example, shift jumper R132 to R133, R134 to R135, and so on.

4.6 USB

One full USB-C port is available through the HD3SS3220 port controller. The USB OTG 2.0 port is directly connected to the GenioSOM. Additionally, three USB debug ports are provided via the FT232 USB-to-UART controller.

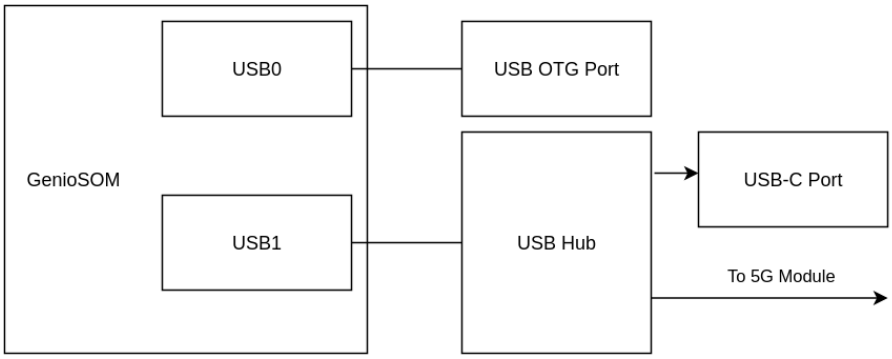


Figure 19: GenioEVB USB diagram

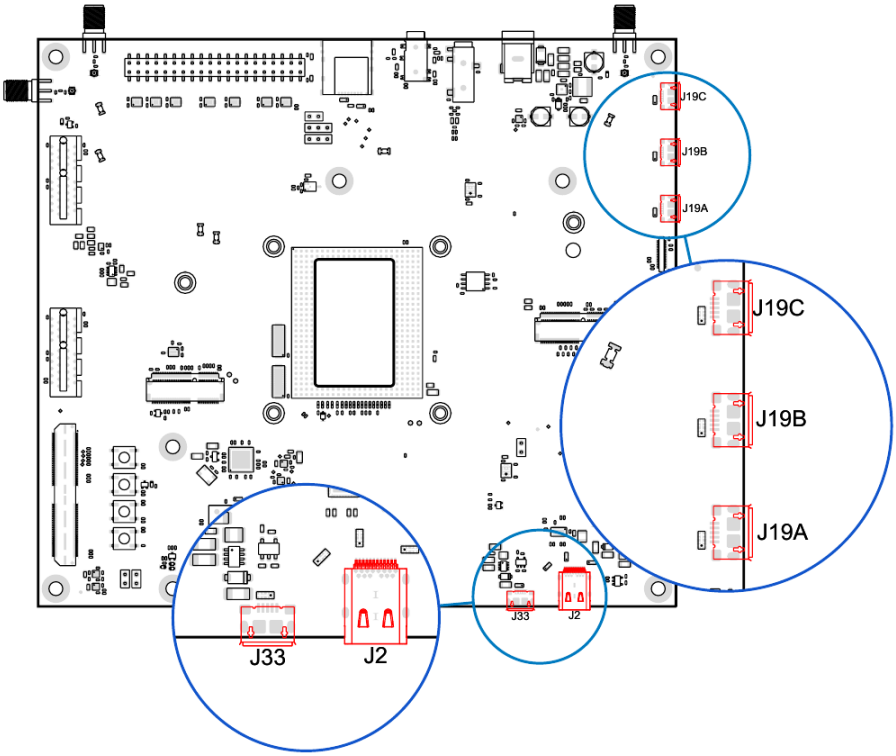


Figure 20: GenioEVB USB connectors

Table 23: GenioEVB USB-to-UART

USB Receptacle	USB Interface	UART Interface
J19A	USB to UART1	UART0
J19B	USB to UART2	UART1
J19C	USB to UART3	UART2

UART2 can be disconnected from the USB-to-UART3 interface and instead connected to the Raspberry PI HAT connector through jumpers J17 and J18.

5 Boot options

The GenioEVB can be booted from eMMC or, if a suitable one is placed on the PCB, from NOR flash. Flashing is performed via the micro USB (J33) port using the Mediatek genio-flash tool.

5.1 Supported OS

The GenioEVB supports a custom Linux Yocto build. To obtain access to the Git repository, please contact `support@grinn-global.com`.

5.2 Flashing

To flash the GenioEVB, one needs a Linux or Windows host PC with AIoT Tools installed, a power adapter, and a micro USB cable.

Here's a high-level overview of the process:

- Connect the Board: Use the power adapter to power the board and connect the board to the host PC via the micro USB port.
- Launch the Flash Tool: Navigate to the directory containing the image files and run the `genio-flash` command with the necessary device tree blob overlays.
- Enter Download Mode: Follow these steps:
  - Press and hold the Download (S3) button.
  - Press and release the RST (S2) button.
  - Continue holding the Download button until the "Erasing 'mmc0" message appears in the log.

For a more detailed description of the process, please refer to the flashing instructions for the corresponding Mediatek Genio 700 EVK: `https://mediatek.gitlab.io/aiot/doc/aiot-dev-guide/master/sw/yocto/get-started/flash/flash-g700-evk.html`

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 24: GenioEVB absolute maximum ratings

	Minimum	Typical	Maximum	Unit
Supply voltage	11.5	12.0	12.5	V
Supply current		4		A
Operating ambient temperature	0	25	70	°C

7 Revision History

Revision	Date	Changes
1.0	23.06.2024	Initial revision.

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